QUALITY & RELIABILITY

Reliability of Various Size Oxide Aperture VCSELs

First published in Proceedings of 52nd ECTC

ABSTRACT

This paper presents AOC's most recent work on 850-nm oxide aperture vertical cavity surface emitting laser (VCSEL) reliability. The VCSELs studied have a range of aperture diameters from about 5 to 20 µm and the reliability effect of aperture diameter is of principal interest in this paper. Larger apertures generally exhibit greater reliability. Electrostatic discharge (ESD) sensitivity thresholds of the various oxide aperture VCSELs is discussed, again showing dependence on diameter, with larger being better. Results for humidity exposure are presented. Here we find no aperture size dependence, because none of the tested designs show significant susceptibility to humidity-induced degradation. It is demonstrated that, in addition to end-of-life degradation, VCSELs generally exhibit variation of performance characteristics during the early part of operating life. This often leads to a requirement for device burn-in. AOC's work in the area of wafer stabilization (trademarked under the name STABILAZE, patent pending) is introduced, showing how critical device parameters such as threshold and slope efficiency can be made to be unvarying over the product's life without the need for costly component or module-level burn-ins.

INTRODUCTION

Following the initial indications that reliable oxide-aperture VCSELs are possible [1,2,3], they represent a growing fraction of all VCSELs produced. As they enter into more applications, each potentially requiring different design optimization, it becomes important to explore the edges of the islands of reliability. Not every possible design is equally reliable, and we don't want to wade so far off shore that we drown.

The reliability methodology, philosophy, and caveats described in earlier VCSEL studies [1,4,5,6] are similar here; their importance warrants repeating the most important points. For example, extrapolation to failure is unwise for VCSELs, testing at application conditions as well as highly accelerated conditions is recommended, and it is important to account for wafer and lot variation. Some results from this work may be generally applicable for all oxide-aperture VCSELs, but the characterization and reliability testing described is specifically for AOC devices. Our very limited testing of VCSELs of different manufacture shows a wide range of reliability performance.

Reliability can have multiple definitions, and there is no single measure that can describe them all. In some cases what we mean by reliability is not how long the devices will last when operated as expected, but how long they will last when the unexpected occurs. ESD (and its cousin, electrical overstress, or EOS) and humidity exposure are in this category. The wearout lifetime that is the more typical subject of reliability studies is of a different character entirely; by either measure AOC VCSELs prove robust. From first principles it is clear that they cannot all be equally so, so a range of devices have been tested, with results summarized below. Reliability distributions and acceleration models are formulated for the various sizes of oxide aperture VCSELs, similar to our previous publications for proton-implanted VCSELs. These allow computation of expected reliability at conditions other than the necessarily accelerated test environments.

It is to be expected that VCSELs of different designs and different aperture diameters should exhibit different reliability. As we show below, depending on what is considered the most important operating characteristic, the results may not always be intuitive.

Since device death is not a necessary component of every definition of reliability, simple stabilization of operating characteristics can often be just as important, a point often overlooked. This is a critical point for many array products, where stabilized wafers allow for confident selection of arrays at wafer level, without the deleterious increase of non-uniformity during product use.

OXIDE VCSEL DESIGN: EFFECTS AND TRADEOFFS

In any semiconductor device, there is a complex interplay of performance requirements, layout and technology options, and fundamental physics that constrains the final design. This is definitely the case for VCSELs. Any VCSEL will consist of an active region between two mirrors, disposed one after another on the surface of the substrate wafer. An insulating region will force the current to flow through a small aperture, and the device lases perpendicular to the wafer surface (the "vertical" part of VCSEL). One type, the proton VCSEL—where the insulating region is formed by a proton implantation, dominated the early commercial history of VCSELs. These have been described in detail elsewhere. [5] More recently, the oxide-isolated VCSEL has become available. In this device, shown schematically in Figure 1, the insulating region is formed by partial oxidation of a thin, high aluminum-content layer within the structure of the mirror.

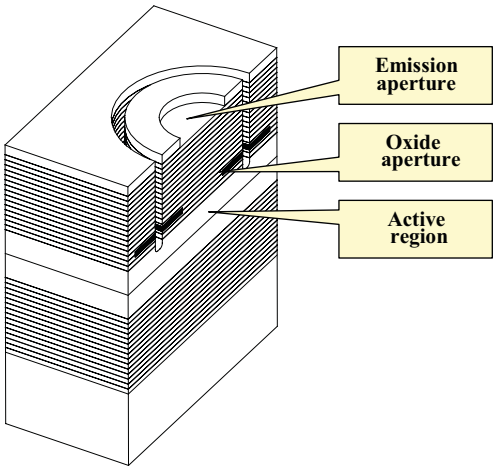

Figure 1. Schematic cross-sectional view of an oxide-isolated VCSEL.

There are a number of obvious design possibilities, such as the oxide thickness, vertical placement, and aperture diameter, as well as many others dealing with design of mirrors, active regions, and doping, all of which can affect the final performance. It is possible to establish a basic design and to produce a wide range of behaviors simply by adjusting the aperture diameters. In particular, the threshold current is generally decreased by decreasing the oxide aperture diameter, but this inevitably increases the device electrical resistance and thermal impedance, because the current must pass through a smaller constriction. As a result, there are inevitable size-related tradeoffs between performance and reliability. Similar decisions must be made about differential efficiency (primarily controlled by top and bottom mirror reflectivity), temperature performance (primarily controlled by alignment of Fabry-Perot cavity wavelength and gain peak wavelength), and speed (controlled by many factors). There is no single best VCSEL!

RELIABILITY RESULTS

One of the primary reasons proton implanted VCSELs have been commercially successful is their outstanding reliability performance over the competing edge-emitting lasers. Because reliability is so critical for VCSEL users, there has been understandable concern about the reliability performance of the newer oxide VCSELs. As with many issues, this one does not have a simple answer. Oxide VCSEL manufacturers employ designs with significant differences in the epitaxial structure as well as thickness, sizing, and placement of the oxide aperture layer. AOC reliability testing, both on a variety of

internal designs and on competitive products, has demonstrated a wide range of reliability results for different oxide VCSEL designs. These differences can affect reliability either by changing the magnitude of the effect of failure modes, or by introducing new ones, such as mechanical stress due to shrinkage on oxidation and to differential thermal expansion of the oxide relative to the semiconductor material. Failure modes such as these can be insidious, as they may not be seen in high-temperature life tests. [1] For these reasons, oxide VCSEL reliability must be assessed for each particular oxide design, and the reliability effects of design choices must be understood through extensive reliability testing.

As with proton VCSELs, AOC continues to emphasize reliability performance for its oxide VCSEL products. By systematically testing numerous design options through statistical experimentation techniques, we understand the reliability impact of such choices. Beyond life tests of the type described here, AOC continues its reliability process monitoring protocols. These include qualifying each wafer for production use by assessing its parametric stability and long-term reliability through sample life testing, as well as quarterly long-term life testing of a sample from production stock. VCSEL users also validate reliability of the AOC VCSEL products (oxide and proton VCSELs); overall VCSEL reliability failures (defined as field failures of any age reported by our customers) were at a 1.3 PPM (6.2 sigma) level for 2001, improved over the 2 PPM reported in 2000. [1]

The reliability results reported here describe the effects of one of the possible design decisions—aperture diameter. As mentioned earlier, each choice may be suitable for a particular application, so there is not necessarily one "best" option. Here we describe the data to assess the reliability trade-offs for each product. Note that reliability discussed in this section means device wear-out, or lifetime. Short-term reliability effects are dominated by changes (increase or decrease) in device characteristics, and thus the need for device stabilization—an important topic discussed later. As was the case for AOC's proton VCSEL, we did not see infant mortality or random failure rates of significance during this testing.

The life testing methodology is the same as AOC has described many times before. [6] Multiple wafers representing several epitaxial growth and chip fabrication lots were employed in the study—at least 3 lots for each chip type. Chips were packaged in TO-style devices, subjected to standard production burn-in, and then placed on long-term life testing. Some of the groups were subjected to air-to-air thermal shocks before starting life testing (this did not impact the results). The burn-in was done in dark, forced-air ovens at about ten different combinations of constant temperature and dc current. Periodically the parts were removed from the oven and dc tested at room temperature. As usual, failure is defined as a 2 dB reduction in output power at a fixed current. While the VCSELs usually degraded in a fairly graceful way during life testing (as opposed to sudden, catastrophic degradation), we did not attempt to estimate extrapolated failure times; reported failure times are always for actual failures.

The results of the life tests are summarized below. Note the large number of devices, device-hours, and failures, which lend credibility to the statistics generated from this data. The data reported here emphasizes the 17 µm, 14 µm, and 5 µm diameters, for which we've generated a considerable set of data. AOC has also performed testing on other aperture sizes: 20 µm, 12 µm, and 8 µm diameters; they follow the same general patterns discussed below. Altogether, we have performed reliability testing on over 4,000 oxide VCSEL devices, accumulating nearly 5 million actual device-hours, with life tests continuing.

Table 1. Summary of life test data. Burn-in temperatures ranged from -65°C to +150°C. Device-Hours is the actual number of total device-hours (number of devices times burn-in hours) compiled during life testing, combining all the burn-in current/temperature combinations for each device type. Number of devices tested and failed are also the totals for all burn-in condition combinations.

Oxide Diameter	Life Test Current	Device-Hours	Tested	Failed
17 µm	20-32 mA	3,513,657	2,898	622
12-14 µm	15-30 mA	315,385	409	144
5 µm	3.5-7 mA	884,992	843	387

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FAILURE MECHANISMS

Data for each of the groups fit the same fundamental temperature and current acceleration model we have published previously for our proton VCSELs [4]: an Arrhenius model with an activation energy of 0.7 eV and an additional dependence on the square of the applied current. That the same activation energy applies would be consistent with a single dominant failure mechanism (or combination of failure mechanisms) for all aperture sizes of our oxide VCSEL as well as for our proton VCSEL. (Other investigators also subsequently found this activation energy and current-squared dependence to be the appropriate wearout acceleration model for oxide VCSELs. [16,17])

The ultimate failure mechanism in all cases (both for the oxide and the proton VCSEL) is most likely related to the presence or generation of dislocations. Edge dislocations that traverse the P-N junction move only as continuous loops by glide or climb along fixed crystallographic directions and form dark line defects (DLDs) by generating a high density of deep point defect traps along their path of motion. DLDs are dark because of the compensating and lifetime killing properties of the deep traps. (While it remains true that DLDs of classical appearance—and resulting rapid degradation—are not found in AOC VCSELs, these and the following comments contrast with earlier AOC interpretations. [1,4,5,6] The DLD wearout mechanism and the stabilization model to be discussed below have similar activation energies, but recent careful TEM analysis suggests that dislocations actually control end of life. It remains possible, however, that both mechanisms are effective at the 2 dB degradation level which is a typical failure criterion.)

The laminar structure of the AOC VCSEL confines propagating dislocations entirely to the plane of the active region (quantum wells and barriers). As a result, the only orientation in which they would appear linear is parallel to the active plane—in which orientation there would be no illuminated region to contrast with the DLD. From the top, the only direction in which the degradation can practicably be observed, the VCSEL emission appears either to dim gradually, progressing inward from an edge, or to dim nearly uniformly over the entire area. Neither of these conditions is clearly evident at the 2-dB degradation we use as our end-of-life definition, probably because only a tiny fraction of the outer edge of the active area is involved at that point. They typically become visible only at 90% or greater degradation. It is probably this fact that leads to the remarkable reliability observed in the VCSEL ac characteristics. [4]

Two items are absolutely required for the propagation of a DLD: a dislocation (or surface) traversing the junction and mechanical stress. As a practical matter, minority carriers must also be present. Without minority carriers, the activation energy for DLD motion is enormously increased. [7] If any one of these three items is missing there will not be DLD degradation. Some mechanical stress is inevitable in the VCSEL; even if not present as a residue of processing, stress will arise from thermal gradients induced by operation. Minority carriers are also inescapable consequences of operation.

Dislocations can come from a variety of sources. VCSEL material growth by MOCVD employs low dislocation density substrates, but the dislocation density is not zero and a small but finite possibility always exists that a substrate dislocation will traverse the P-N junction inside the diameter of the isolation implant. The central portion of the cavity is the most vulnerable. Substrate dislocations in the region under the oxide or gain guide implant will have a reduced effect due to the lateral debiasing. Even if a pre-existing dislocation or surface is not accessible in the region of flowing current, they can be generated in situ. Point defects can be generated near the oxidation layer, and the isolation implant produces a high density of point defects that define the perimeter of the P-N junction. Under forward bias, minority carriers that recombine non-radiatively on these point defects impart energy to the defects that allow them to move so as to lower the free energy in the crystal. Aggregation of point defects into a dislocation loop produces a nucleus for DLD propagation and subsequent degradation.

Degradation resulting from grown-in dislocations is generally fairly rapid. In the rare instances where it occurs, it can typically be detected and removed by a short operating burn-in (such as the STABILAZE process described below). Generation of dislocations through aggregation of point defects is much slower; it is this mechanism that likely controls wearout life of AOC VCSELs. While details of VCSEL degradation remain open issues, it involves a combination of the mechanisms above (and perhaps others), and appears to be fundamentally similar for AOC's proton and oxide VCSELs of all sizes.

RELIABILITY MODEL

Modeling the cumulative failure rate with time results in a curve best fit by the lognormal distribution, as we have consistently reported for the proton and oxide VCSEL [1], see reference [6] for a more complete discussion of the lognormal distribution. This distribution is often used to model wearout; contrast that with random failures, typically modeled with an exponential distribution. As in our previous studies we do not see infant mortality or random failures as significant portions of the time-to-failure distribution, we see only a single wearout curve.

Comparing the reliability of different VCSEL types can be done in a number of ways. Figure 2 shows one such comparison, with the assumption of nominal operating current for typical standards-driven high-speed data communications (acceptable power and speed performance requires a different current for each device type). As can be seen, the proton VCSEL and the two largest oxide VCSELs all exhibit remarkable reliability in these conditions, with less than a decade separation between them. Single mode parts inevitably lag somewhat behind.

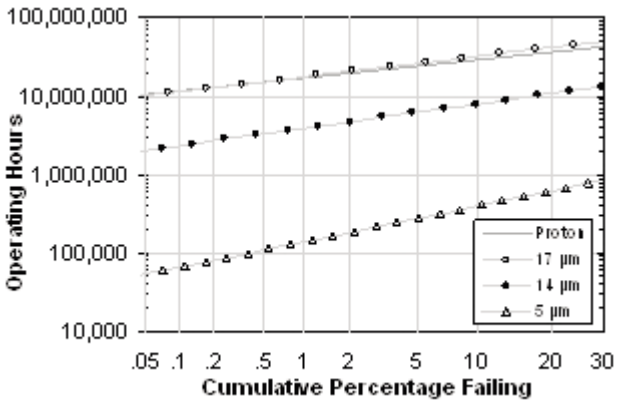


Figure 2. Comparative reliability of different designs at 25°C and nominal operating currents (10, 8, 6.5, and 3.5 mA for Proton, 17 µm, 14 µm, and 5 µm respectively).

The slope (sigma) parameters for these oxide devices appears slightly higher than the proton VCSEL's 0.5—about 0.65, 0.7, and 1.0 for the 17 µm, 14 µm, and 5 µm devices, respectively. This is probably due to a combination of factors related to the influence of process variation. A more uniform process will result in a smaller slope parameter, flattening the curves shown in Figure 2 and thus indicating fewer early failures. Small-aperture VCSELs are more sensitive to process variation; the same absolute difference in, for example, aperture diameter leads to a larger percentage difference for a smaller diameter device. Even so, the sigma parameters for these newer devices will shrink (and median lifetimes increase) as their processes continue to mature. This steady sigma improvement throughout product maturation was demonstrated by our proton VCSEL. [4]

The absolute lifetime for the large-aperture oxide VCSEL is very similar to that of the proton VCSEL, whose current confining structure is of similar area. Lifetimes of the smaller oxide VCSELs decrease proportionally with area, as discussed in more detail below, even when the reduced operating currents are taken into account. Nevertheless, reliability should be assessed against the needs of real-life applications, and for all these devices the models project decades until even a small fraction of the devices fail. Additionally, users of reliability data need to be aware that all models are imperfect—reliability models have particularly wide error bands, due to the necessary compounding of extrapolations from high stress conditions to application conditions of interest. While AOC strives to reduce these as much as possible, through broad sampling and conservative testing and analysis methodologies, the models cannot be taken to be too precise, and the underlying assumptions inherent in the model should be understood.

THE MANY FACES OF VCSEL RELIABILITY

As described above, many VCSEL characteristics can be affected by design choices, and there is not a single "best" VCSEL for all applications. Similarly, there can be many different definitions of reliability. In addition to the available choices of VCSEL technology and geometry, the application may dictate the reliability definition. As an obvious example, if the VCSEL power is continuously monitored and the current adjusted to maintain it, the time to failure must be defined very differently than it would be when a fixed current is set during manufacture and the resulting power is expected to be maintained over life. In many cases, power is not even the key variable; in many data communications applications modulation characteristics such as extinction ratio and turn-on delay are much more important. [14] Finally, the operating point may influence reliability in perverse ways. The simplest illustration of this point is that a VCSEL operated only 1 mA above its threshold current will degrade much more slowly

than the same device operated 10 mA above its threshold. However, the power effect of a degradation-induced threshold increase of 0.9 mA is less than 10% in the latter case, but it is 90% in the former!

There may be a performance characteristic of overriding importance that forces the choice of a particular VCSEL type, independent of reliability. If, for instance, lowest possible operating current is more important than highest possible maximum power, the smallest-diameter device may be necessary, and reliability implications must be understood and designed for. Whether the reliability of the small device is greater or less than that of a larger device, and by how much, depends on many factors. While a complete catalog of such factors would vastly overinflate this paper, some are illustrated in the figures below. (All graphs show the proton VCSEL for reference, and three oxide VCSEL diameters. The plotted variable is time to 1% failures, based on the models developed above.)

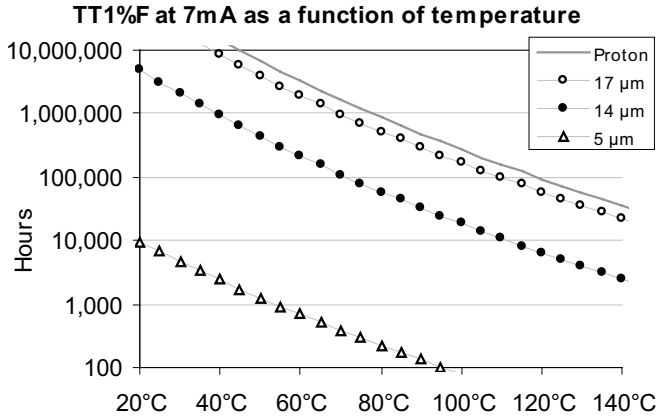


Figure 3. Reliability as a function of ambient temperature at a fixed current.

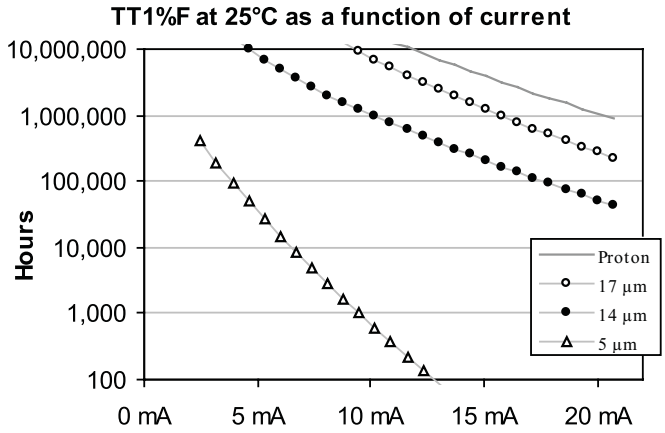


Figure 4. Reliability as a function of current at a fixed temperature.

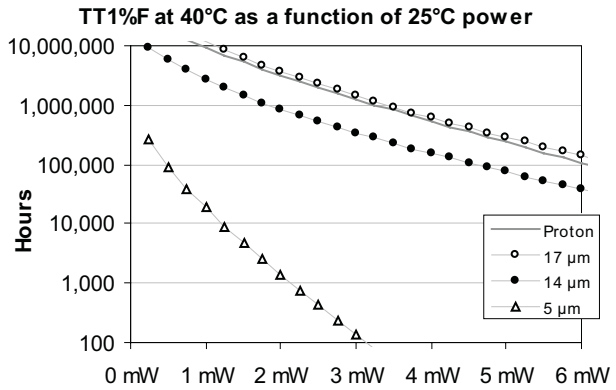


Figure 5. Reliability as a function of emitted power. The reliability is calculated at 40°C, but based on the current necessary to achieve the stated power at 25°C. Note the inversion of which device is most reliable compared to the previous figures.

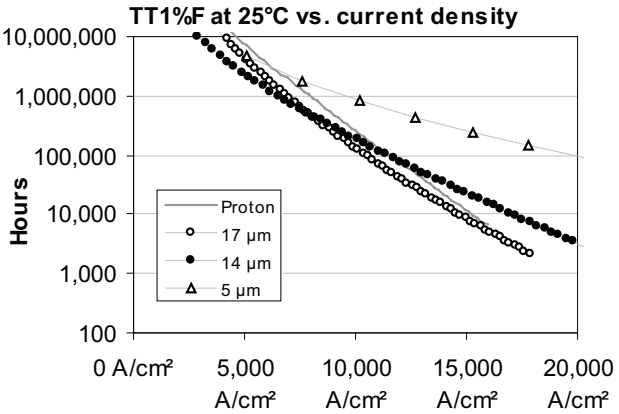


Figure 6. Reliability as a function of current density. Despite having lowest reliability at typical operating levels, smallest device is actually disproportionately more reliable in this physically fundamental sense.

By every measure described above, 5 µm VCSELs have the worst reliability. After adjusting for area, however, Figure 6 shows that small devices are not fundamentally inferior. Possibly as a result of the greater ratio of aperture diameter to outer conducting boundary diameter, at constant current density small devices are generally superior.

Finally, a look at operation in an entirely different regime. When a current pulse is very short relative to the effective VCSEL thermal time constant—about one microsecond—the junction does not have time to heat, and very high peak currents and peak powers are possible. As Figure 8 shows, lifetime at a fixed duty cycle can be quite variable with frequency.

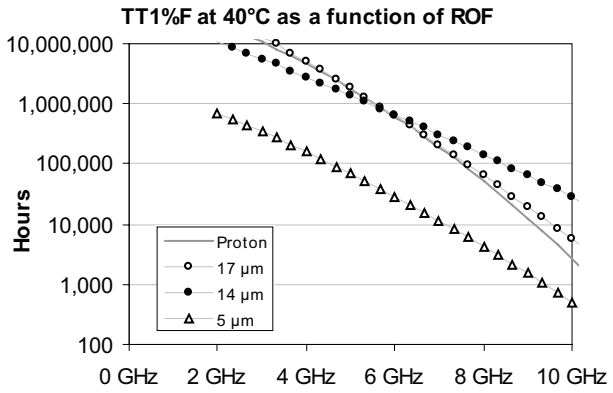


Figure 7. Reliability as a function of Relaxation Oscillation Frequency. This is a fundamental measure of likely modulation performance; it depends on the square root of the ratio of stimulated current to threshold current. The medium-sized oxide is most reliable by this metric.

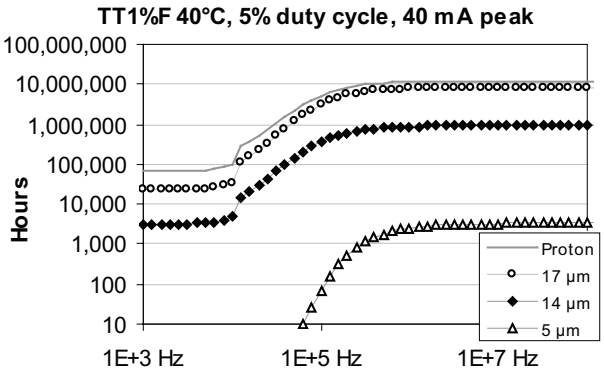


Figure 8. Calendar reliability as a function of repetition frequency for pulsed operation at a fixed duty cycle and peak current. For the same average power dissipation, reliability can vary over three orders of magnitude.

HUMIDITY EFFECTS

In applications using non-hermetic packages, such as arrays and low-cost VCSEL sensors, the reliability effects of humidity exposure are critical. AOC has used a range of tests to understand the behavior of its oxide VCSEL when exposed to humidity, and found all sizes of its oxide VCSEL to withstand humidity quite well. The traditional humidity test is 85ºC and 85% relative humidity, a test we performed. However, as this is an unusually harsh test, so accelerated that 2000 hours exposure can be estimated using standard humidity models [8,18] to be the equivalent of nearly 30 years at normal operation, we have also included some testing at the more reasonable 65ºC, 65% relative humidity. We also addressed the question of whether operational (biased) humidity testing is harsher than humidity storage (unbiased) testing—we did both. Although some electrochemical corrosion failure mechanisms will be accelerated through bias, our past data has indicated that unbiased may actually be worst case, because when bias is applied the device's small self-heating reduces the local relative humidity.

Oxide Diameter	Condition	Device-Hours	Tested	Failed
17 µm	85/85 storage	58,753	27	0
	85/85 operating	24,111	9	0
	65/65 storage	61,432	28	0
	65/65 operating	26,790	10	0
12-14 µm	85/85 storage	8280	12	0
	85/85 operating	7590	11	0
5 µm	85/85 storage	79,000	45	0
	85/85 operating	71,500	61	0

Table 2. Summary of humidity test data. Device-Hours is the actual number of total device-hours (number of devices times exposure hours) compiled during testing.

Devices were built from a range of oxide VCSEL lots and packaged using windowless TO cans for atmospheric exposure to this humidity testing. Test protocols and failure criteria were the same as described earlier, with the additional step of an unbiased dry bake immediately prior to and following exposure to the humidity, to avoid condensation. Table 2 shows the results of this testing; most groups have exceeded 1000 hours of humidity exposure. No failures were found, so we are not able to ascertain any dependence on aperture size. These excellent results indicate that no terrestrial application appears out of bounds for AOC's oxide VCSEL. As with reliability, humidity resistance is not necessarily the same for all oxide VCSEL designs, so users need to carefully validate the particular design chosen.

ESD VERSUS APERTURE SIZE

ESD damage can cause early life or "infant mortality" VCSEL failure. ESD testing was done MIL_STD-883D, Method 3015.7 Human Body Model (HBM) conditions. Samples (typically 5 units) of 5-20µm aperture diameter were step stressed in voltage. Three pulses, forward and reverse, were applied at each stress voltage, with one second delay between pulses. Failure was defined as –2dB change in optical output power, and damage threshold defined as a measurable (>3%) change in optical output power. It is worth repeating here that at somewhat lower voltages even if patent damage is not evident that latent damage may severely compromise operating life. [4]

The measurement results are plotted as a function of oxide aperture diameter in Figure 9. ESD damage is expected to be a function of the oxide aperture area and/or diameter. The data only approximately fits a linear function (appropriate if the effect is controlled by spreading resistance) or a parabola (appropriate if controlled by cylindrical resistance). The 5-µm part is somewhat more robust than either model would predict, probably for reasons similar to those advanced to explain Figure 6 above.

The oxide VCSEL ESD sensitivity is similar to proton VCSEL values for similar aperture diameter, and dictates similar careful ESD controls. Susceptibility increases inversely with aperture diameter, requiring increasingly rigorous ESD controls in handling to assure reliable application operation. Using the maximum aperture diameter appropriate for the application is highly desirable.

Human Body Model (HBM) is one ESD test method. There are other ESD test methods, including Machine Model (MM) and Charge Device Model (CDM). For some of these models sensitivity measurements on proton VCSELs have shown much lower voltage damage levels, with similar results expected for oxide VCSELs.

Electrical overstress (EOS) is a close cousin of ESD, and can also damage VCSELs, as dramatically illustrated in figure 10. While we have not done a specific comparative study of the effects of EOS for the different oxide VCSEL products, it is reasonable to expect the same effect as for ESD exposure; that is, the smaller aperture device is more sensitive to the effects of electrical overstress.

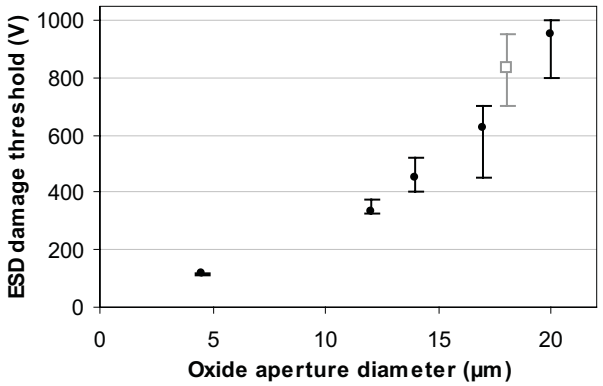


Figure 9. Dependence of patent ESD damage threshold on aperture diameter. Dot shows voltage at which the typical part exhibits degradation, bars indicate first and last parts degrading. Gray square and bars show proton VCSEL for comparison.

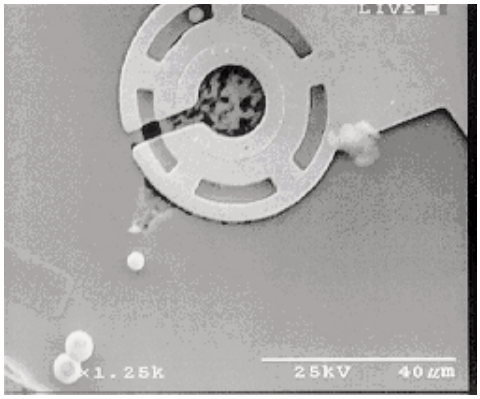


Figure 10. If only they were all so easy to diagnose! VCSEL subjected to EOS which explosively melted material in the active region and under the contact, depositing ejecta some distance away.

THEORY OF VCSEL PARAMETER STABILIZATION

As will be explained below, powered operation is the last step in any VCSEL wafer fabrication process. In some combinations of application and operating condition it may be acceptable for this step to occur in the application itself. For most, however, it will occur at an intermediate process. Whether it occurs in the application, at a subassembly process, or at the wafer level, it produces internal re-structuring in the VCSEL, justifying the opening comment. For well-made VCSELs, burn-in is not primarily a screening device intended to remove "infant mortality" (though it can serve that function as well). It is rather the method by which the remarkable stability that is one of the VCSEL hallmarks is established.

Below threshold any laser diode is merely a diode. In particular, laser diodes below threshold are inefficient LEDs. At threshold the round-trip gain in the cavity is constrained to a value of 1.0, essentially clamping the quasi-Fermi levels at the P-N junction. All current above threshold goes into stimulated emission and produces the coherent laser output. Any change in the applied voltage above threshold value is essentially due to the series resistance.

These are important considerations for laser diode reliability because the currents and voltages in the vicinity of the P-N junction are all determined by the LED diode characteristic just below threshold.

III-V semiconductor diodes typically exhibit two components of current. The minority carrier injection and recombination current that produces light output has an exp(qV/kT) characteristic. The Sah-Noyce-Shockley [9] (SNS) depletion

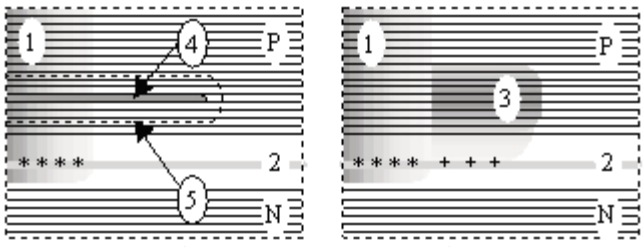
layer recombination current has an exp(qV/nkT) characteristic where 1.3<n<2.0. For 850nm AlGaAs diodes n~2. For double heterostructure P-N junctions the "2kT" SNS current is essentially present only at the junction perimeter and the "kT" minority carrier recombination current is present over the area of the junction.

Some LEDs employ a high lateral sheet resistance layer next to the P N junction that debiases to the perimeter. By this means the central region of the junction operates at full current density for light generation but the junction perimeter operates at a much lower current, improving both performance and reliability.

A lateral debiasing structure similar to that used in LEDs is included in all VCSELs. The conductive P-type material below the current-guiding insulating layer provides the lateral debiasing which assures that the junction perimeter is operated at a lower current density than the central region. This is true whenever a current constricting insulating layer is provided, whether by a "gain-guide" proton implantation, by an oxide layer, or by any other means.

In the VCSEL the junction perimeter is defined either by an actual surface or by an isolation implant. Either the real surface or the isolation implant produce "2kT" current at the junction perimeter.

Figure 11, an enlarged portion of Figure 1, schematically shows the location of the oxide layer and proton implants in typical VCSEL structures. Figure 11(a) represents an oxide VCSEL and Figure 11(b) represents a proton VCSEL. The right hand edge of the two figures represent the center line of the optical cavity; the VCSEL cavity has radial symmetry. The deep shaded area (1) in both figures represents the multi-energy isolation implant that in this design converts the material to semi-insulating from the top surface to a depth below the quantum wells. It could be replaced by an etched edge with no change to the subsequent analysis. The quantum well



(a) Oxide (b) Proton

Figure 11. VCSEL current confinement structures.

region, which contains the P-N junction, is represented by the gray stripe (2) between the two white bands representing the P- and N-type spacer layers that set the cavity length of the VCSEL. A portion of the P-type Bragg mirror is shown on the top of each figure and a portion of the N-type Bragg mirror is shown on the bottom.

The depth and range of the gain-guide implant in proton VCSELs is represented by the gray area (3) in Figure 11(b). The high lateral sheet resistance below the gain guide gives excellent debiasing of the P-N junction at the isolation implant perimeter.

While proton implant simulations do not predict a significant concentration of defects in the quantum wells for the implant energy used, a significant "nkT" current is found in the area under the gain guide implant. The SNS current at the junction perimeter has n = 2; the recombination centers responsible for this current are represented by (*). For the area under the gain guide implant the SNS current has n = 1.85.

The presence of the "1.85kT" current and the loss of radiative efficiency shows that a significant concentration of point defects is present in the annular region of the junction under the gain guide implant. The location of these point defects is represented by (+) in the quantum well region under the gain guide implant in Figure 11(b). Neither of these effects is seen in the central region of the cavity inside the gain guide implant aperture.

In oxide VCSELs the wet thermal oxidation process forms an annular ring of aluminum oxide represented by the dark gray layer (4) in Figure 11(a). The oxidation process also removes acceptor concentration from the equivalent of six mirror periods plus the oxide thickness as illustrated by the dotted region (5) around the oxide layer in Figure 11(a). In this case, the sheet resistance of the P-type layer under the oxide is a function of the thickness and placement of the oxide layer relative to the quantum wells.

All AOC VCSEL wafers have five process monitor test sites that are used to monitor important parameters of the material and process. Among the recorded parameters that have an impact on VCSEL reliability are sheet resistances at various locations within the vertical structure and "nkT" values at various locations within the lateral structure.

It was analysis of process monitor tests that revealed the important aspect of the oxidation process shown as (5) in

Figure 11(a). A defect is being generated in the oxidation and diffusing into the surrounding P-type mirror layers for an effective distance of about 400nm; this defect compensates the acceptors. The acceptor compensation can be removed with a high-temperature anneal immediately following the oxidation. For the wet thermal oxidation process, hydrogen is a likely candidate for this defect.

Other investigators [10, 11] have found a dramatic reduction in lifetime near the semiconductor/oxide interface to a depth of 150Å that is attributed to excess arsenic generated by the oxidation process. This is thought to be similar to the surface pinning observed in arsenic based III-V semiconductors. [12,13] The compensated region reported here is in addition to the low lifetime observed at the oxide/semiconductor interface.

The test structures in the process monitors also show that there is no "nkT" current under the oxide layer—with or without annealing. The absence of the area "nkT" current under the oxide layer is one of the reasons oxide VCSELs have lower threshold current than proton devices.

VCSELs typically incorporate considerable hydrogen. It can originate in epitaxy, in proton implantation, or in oxidation. As an interstitial donor, hydrogen is a highly mobile species that tends to compensate the shallow acceptors in the P-type mirror layers. Hydrogen can be partially removed by high temperature anneal before wafer processing. Many hydrogen impurities are introduced into the device structure late in the process, however, when significant thermal annealing is not possible because of deleterious effects on intentional structures.

The presence of this hydrogen and other mobile point defects (all of which will be called hydrogen below) has made it necessary to perform a burn-in on both oxide and proton VCSELs to stabilize their characteristics. The stabilization burn-in is performed at elevated temperature and high bias current. These conditions set up the thermal and electrical bias fields similar to those present in an operating VCSEL, and insure the presence of minority carriers. Under these conditions the hydrogen and other mobile defects coalesce or move to a final distribution so that the long term variation in performance is minimized. During the burn-in, multiple simultaneous effects can change threshold current and other important characteristics.

Interstitial hydrogen has an affinity for certain acceptors and tends to migrate to the site of the acceptor and form a hydrogen-acceptor complex. [14] When hydrogen diffuses into the conducting region just above the quantum wells it will compensate the acceptors and cause the sheet resistance to rise. An increase in lateral sheet resistance under the oxide will result in more rapid radial debiasing and a decrease in threshold current.

The ionized interstitial hydrogen atom forms a positive ion in the semiconductor lattice. The polarity of the electric field under operating bias will cause unpaired hydrogen to drift toward the junction perimeter. S. Shi [10] reports that hydrogen decreases the surface recombination velocity at an oxide/semiconductor interface. This ability of hydrogen to neutralize surface states probably also applies to the damage centers produced by an isolation implant. Hydrogen drifted to the junction perimeter during the stabilization burn-in can reduce the "2kT" current by neutralizing the deep traps and bring about a decrease in threshold current.

In a similar manner, hydrogen that diffuses into the quantum well region can neutralize the "nkT" non-radiative centers under the gain guide implant. This will also cause a decrease in threshold current.

The elevated temperature and high minority carrier concentration present during the stabilization burn-in can cause hydrogen to be removed from the active region of the VCSEL. H. Fushimi and K. Wada [14] indicate that the presence of minority carriers and elevated temperature can facilitate the dissociation of acceptor-hydrogen complexes. Diffusion and drift of the unpaired interstitial hydrogen donors into the surrounding isolation implant region will cause the lateral sheet resistance of the conducting layer under the gain guide implant or oxide to decrease. A decrease in lateral sheet resistance means that a larger portion of the P-N junction is biased to a higher "kT" current density. Thus, even if the "nkT" and "2kT" currents are decreased, less debiasing in the lateral junction can cause the threshold current to increase.

The relative contributions of these and other mechanisms vary from design to design and from process to process. The one constant is that some change is typical during initial operation of a VCSEL. If the application is sensitive to such changes, the VCSEL must be stabilized before it is employed in the application. This is true even when, as is typical in the case of AOC VCSELs, early degradation failures are extremely rare.

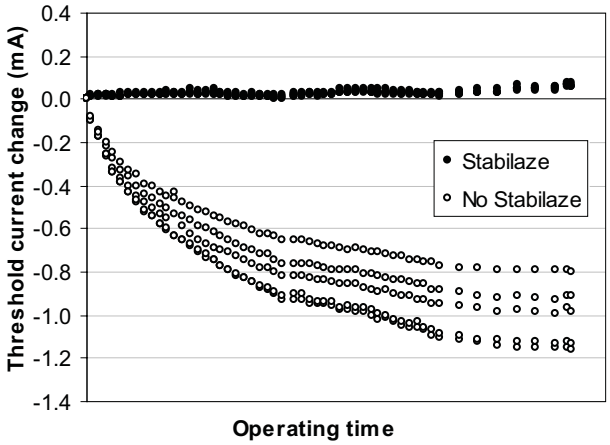


Figure 12. Change in threshold current during operation for ten parts from two wafers. The wafers were identical, except one had been through the STABILAZE process and one had not. The parts without STABILAZE change significantly during initial operation but are stable thereafter.

WAFER-LEVEL STABILIZATION AND STABILAZE

STABILAZE is the trademarked AOC VCSEL wafer-level stabilization process. It conditions critical VCSEL device parameters at wafer level to be unvarying, duplicating the results of and eliminating the requirement for subsequent package level burn-in, thereby improving cost efficiency and making wafer level selection of key parameter uniformity (for array product applications) practical.

Figure 12 illustrates why stabilization is so important. Unless the VCSEL is subjected to a burn-in of some sort prior to shipment, it may take minutes, days, or weeks for the operating characteristics to reach their final values. The magnitude of the changes depends on the specific VCSEL design and on the operating conditions. The devices in Figure 12 have an unusually high amount of variation during early operation; this was a result of a design tradeoff in which a particular final operating characteristic was optimized at the expense of short-term variation. It is always possible to do a stabilization burn-in at a later assembly stage, but it is almost always less desirable to do so—only partly because it is more costly.

The STABILAZE process was developed and optimized to provide equivalent or better results to package level stabilization burn-in. Equipment, materials, and process techniques were defined to contact, without damage, all dice across the wafer for uniform bias current and uniform wafer temperature. A mechanically compressible, electrically and thermally conductive contact material was identified to provide contact without mechanical damage. High thermal dissipation (>2000 watts/wafer) was a key equipment requirement. Device design was refined to assure wafer level bias current flow duplicated package level operation. Extensive characterization and reliability testing on many (hundreds of) wafers verified short term stabilization and long term reliability, using the wafer by wafer qualification process described in reference [6] and accelerated burn-in testing at 100-150?C to compare failure rates with existing device reliability models.

The utility of full-wafer mapping of test results, and the tool AOC uses for the purpose, have been described previously. [4,15] The use of color to represent relative values and the ability to re-scale the data to highlight small differences can lead to revelations that would never be possible with statistical summaries of component-level data. One such profound revelation came when maps from before and after the STABILAZE wafer-scale burn-in process were compared. While the total standard deviation of the data was essentially unchanged, the distance scale over which variation occurred was markedly reduced. Patterns with a scale as small as a few hundred microns appeared, superimposed on the longer-range variation previously known to result from epitaxial and processing gradients. Examples are shown in figures 13, 14, and 15. The magnitude of variation is often small, but the patterns are very real. These small-scale patterns may have significant implications for VCSEL arrays—if we used only the wafer data from before STABILAZE and subsequently burned in an array component, the uniformity would be compromised. If this happens late in an assembly process, the cost is enormously greater than if it can be detected and removed at the wafer level.

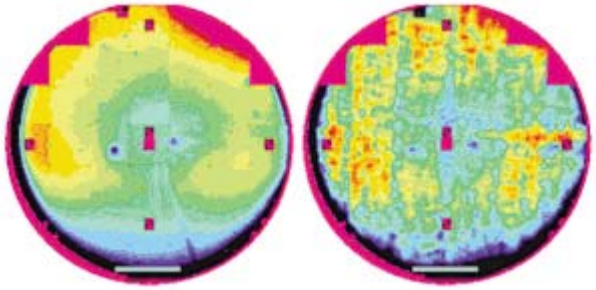


Figure 13. Full wafer maps of forward voltage, before (left), and after (right) STABILAZE processing. Note the significant increase in short-range variation.

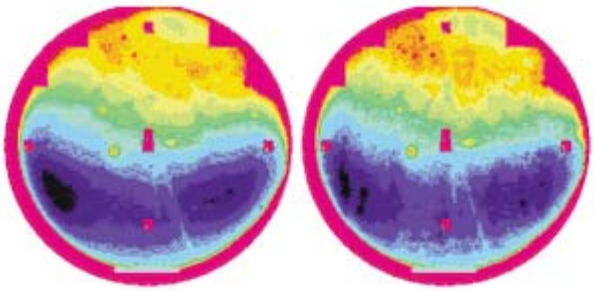


Figure 14. Full wafer maps of threshold current, for the same wafer as in Figure 13. As in the case of forward voltage, short-range variation increases.

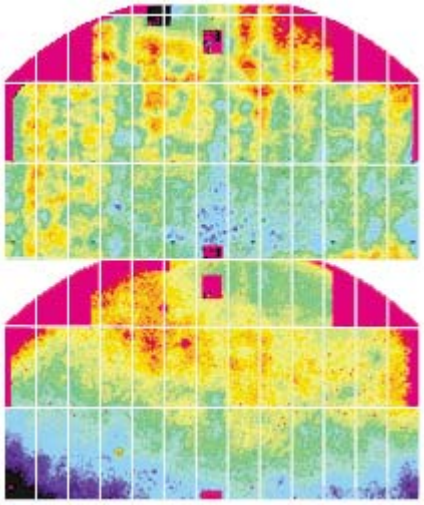


Figure 15. Enlarged views of post-STABILAZE forward voltage (top) and threshold current (bottom), showing topological similarity.

The detection of patterns in the test results leads to an obvious question: After the stabilization process, do the different regions also exhibit different reliability? As the experimental results of Figure 16 show, the answer is clear: they are all equally reliable. Thus we can be comfortable that after stabilization the uniformity will not be further degraded during the operating life

Another obvious question is whether the patterns observed after STABILAZE are a fundamental result of burn-in, whether at wafer or component level, or are exclusively a quirk of the STABILAZE process. This is more difficult to answer, because the patterns often involve only subtle differences in the measured parameters, and measurements after packaging are susceptible to significantly more variables than are those performed on-wafer. While these variables make it difficult to call the results conclusive, we performed an experiment that suggests the patterns are inherent in the burn-in response of

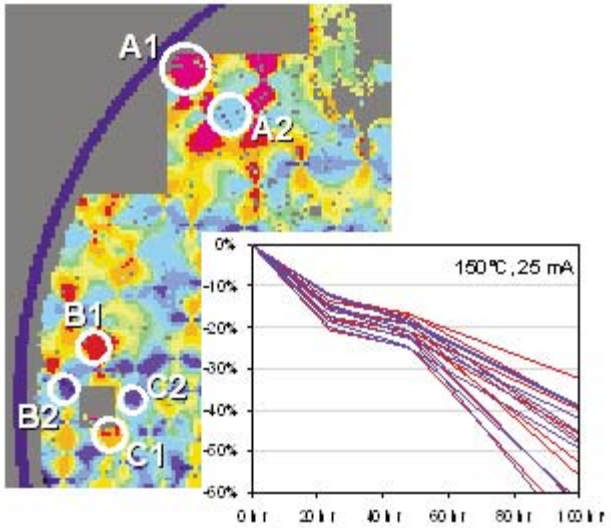


Figure 16. Experimental demonstration that long-term reliability of devices selected from either high- or low-value regions of STABILAZE-stabilized wafers is the same. Samples were selected from each circled region and burned-in as components at the extremely stressful condition shown. The lifetime is essentially the same for all devices.

the wafer, regardless of when or how that burn-in is performed. Keeping careful track of the originating location on a wafer that had not undergone STABILAZE, we assembled 748 individual VCSEL chips into TO packages. These packaged devices were burned-in and tested; then the results were placed in X,Y sequence so they could be compared in map form to the wafer probe data. Figure 17 shows the result of the comparison for forward voltage at 2 mA. There is a clear level shift and a significant increase in small-scale variability.

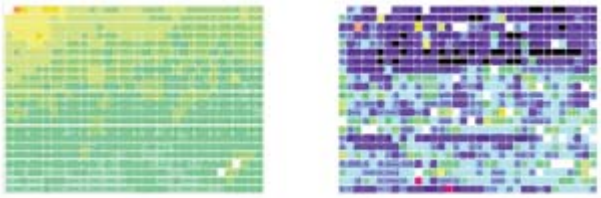


Figure 17. Comparison of forward voltage measured on-wafer, before any burn-in (left), and in TO-components after burn-in (right). Both the average level and the small-scale variation change.

While speculation is possible, the source of topological variation in post-burn-in distribution of VCSEL performance characteristics is not known. Given the difficulty of its detection, its elimination may not be practical. Regardless, in those applications most sensitive to its consequences, they can be minimized by powered operation followed by careful testing.

CONCLUSIONS

AOC's extensive reliability work for its proton VCSEL has been extended to several varieties of its oxide VCSEL. All this testing pays off—the parametric and reliability effects of the design space are now well understood. Reliability testing for large (17 ?m), medium (14 ?m), and small (5 ?m) diameter oxide apertures shows that the larger device generally gives better reliability for expected application currents. However, different conclusions may be reached depending on the parameter of greatest importance. So reliability is in the eye of the beholder, who should also understand the assumptions underlying reported reliability models, as they can dramatically affect the conclusions reached. Neither infant mortality nor random failure appear to be a significant issue in our well-controlled tests; however, smaller aperture VCSELs have much lower thresholds to ESD which may lead to random failures due to improper handling. Humidity resistance is excellent for all sizes of AOC's oxide VCSEL. Finally, a key component of VCSEL reliability is ensuring parameters remain stable over time (distinct from degradation). While in the past this has typically been achieved through component-level burn-in, AOC has now developed the STABILAZE process, which stabilizes the VCSEL parametric performance while still in wafer form.

So through painstaking study of both short-term variation and long-term reliability, AOC has been able to develop the appropriate design boundaries and process windows to achieve stable, reliable oxide VCSELs of several types to serve the various user needs. This is only possible by combining statistical experimentation techniques like design-of-experiments with production-scale analysis tools such as wafer maps to study a wide range of designs. It is crucial to explore the design possibilities, not just the design that will be the final product, before these islands of reliability can be fully defined.

ACKNOWLEDGMENTS

The authors wish to acknowledge the contributions of Mike Haji-Sheikh, MiCha Hatfield, Simon Rabinovich, and Fred Winn.

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