

50Gb/s Per Lane Electrical I/O Optics Design Considerations

Session 3-TU1: The Role of Signal Integrity Practices
in Optical Design Qualification

DesignCon 2015

Santa Clara, CA

27 January 2015

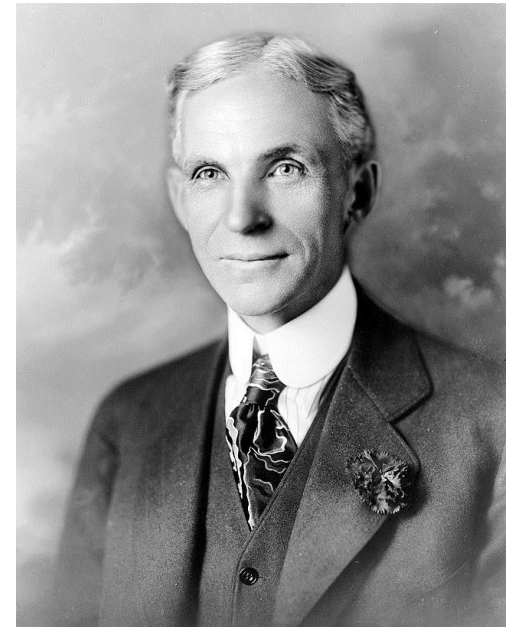
Chris Cole



Finisar[®]

Supplier Preference Example

“Any customer can have a car painted any colour that he wants so long as it is black.”

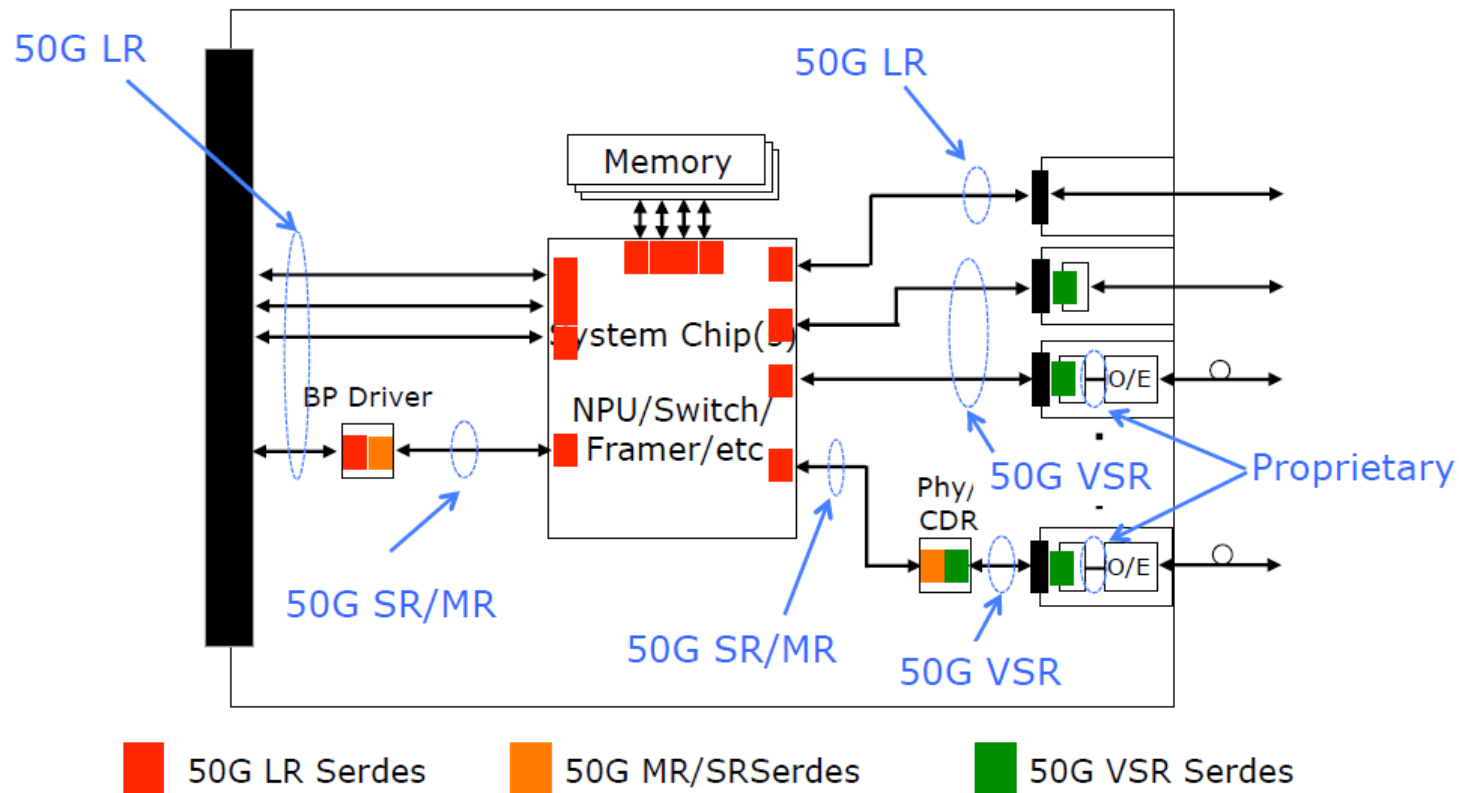


Remark about the **Model T** in 1909, published in **Henry Ford** autobiography “My Life and Work” (1922) Chapter IV, p. 71

Customer Preference Example

- Technology (ex. SerDes) per lane rate Gb/s:
1 → 2.5 → 5 → 10 → 25 → **50**
(black designates existing and blue designates new rates)
- IEEE Ethernet Router & Switch MAC rates Gb/s:
0.1 → 1 → 10 → 100 → **400** → **200**
- IEEE Ethernet Server & Switch MAC rates Gb/s:
0.1 → 1 → 10 → 40 → **25** → **2.5** → **5** → **50**
- Why are there so many new data rates?
- Why not just follow the historical progression, develop 1Tb/s Ethernet and be done with it?
- Because matching the application data rate to the best available technology rate results in cost and performance optimized solution for the customer

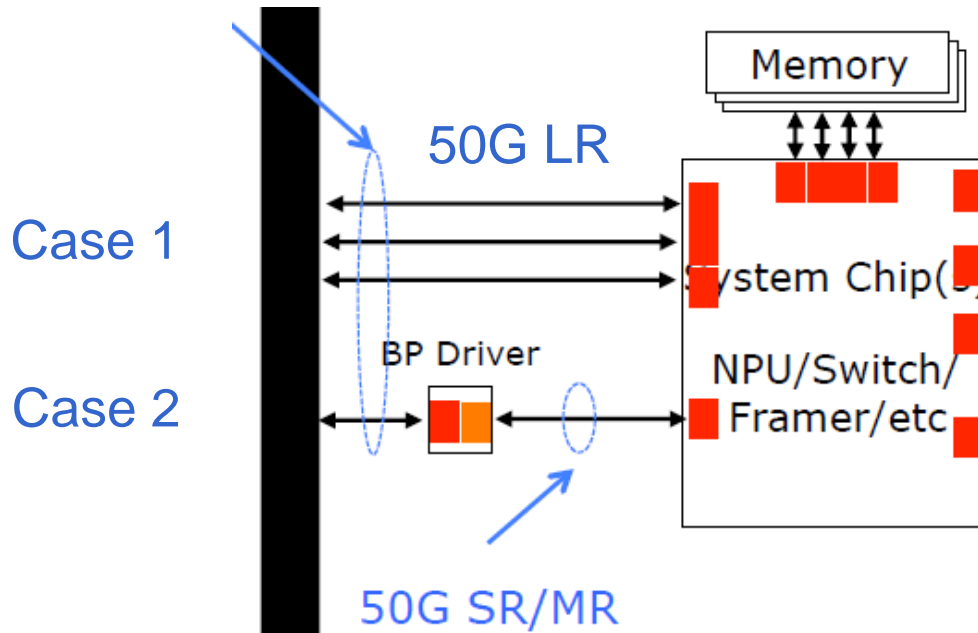
Supplier Preference for 50G Host Card



“Value of Common Electrical Modulation Scheme for CDAUI-8 (8x50G) from a System Perspective”, Gary Nicholl, Joel Goergen, et. al, IEEE 400G Ethernet Task Force, Jan. 2015.

Translation: You can have any 50G modulation so long as it is PAM4

Reality Check: Backplane

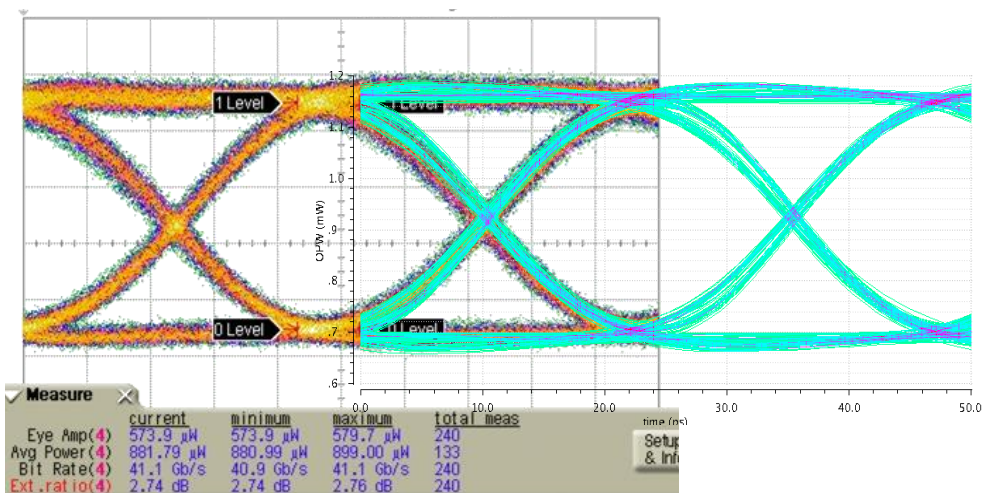


- Link Power:
 - Case 1: 2x (ASIC LR) SerDes (if feasible)
 - Case 2: 2x (ASIC LR + Driver SR + Driver LR) SerDes
- SerDes that supports LR channel directly (Case 1) results in excessive power for SR channel and Case 2 total
- Memory also does not need LR SerDes

Reality Check: Embedded Optics and Si PIC

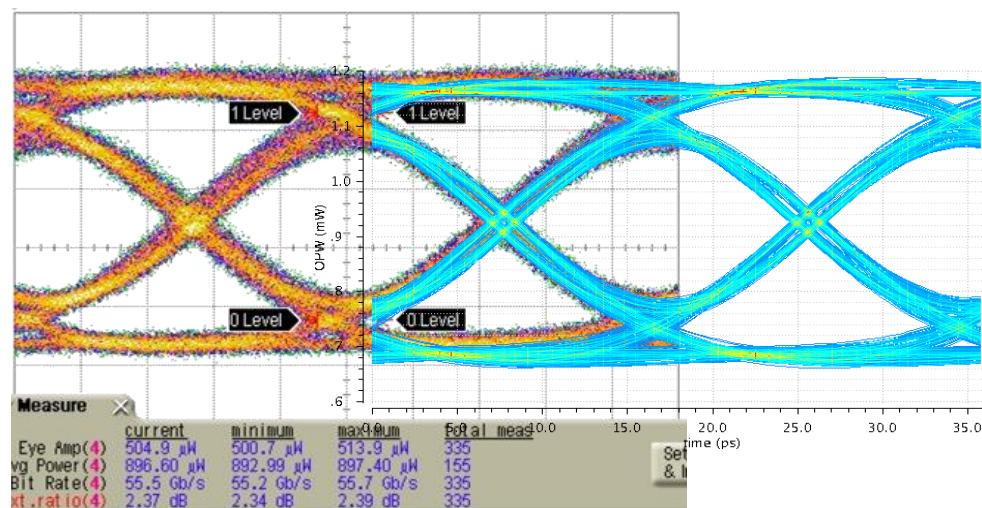
- Embedded Optics (short reach) Interfaces:
 - XSR: ASIC to board mounted Optics interface
 - USR: ASIC to co-packed Optics interface
 - Not considered in Common Electrical Scheme
- XSR and USR channels are easily supported with simple, low power NRZ I/O
- Si PIC Strength: Bandwidth
- Si PIC Weakness: TX power, RX sensitivity
- PAM-4 has ~3dB optical link budget penalty vs. NRZ
- NRZ plays to Si PIC strength
- PAM-4 plays to Si PIC weakness

50G NRZ SiP PIC TX Data Example



40Gb/s, PRBS9 TX
optical eye diagram at
 $\pi/2$ bias:

- Measurement data,
- Simulation



56Gb/s, PRBS9 TX
optical eye diagram at
 $\pi/2$ bias:

- Measurement data,
- Simulation

Finisar 2x50G hybrid SiP PIC fabricated at ST Microelectronics

Future Electrical I/O Design Considerations

- Standards Based
- Proprietary
- 50G PAM-4 for general purpose host card designs
- 50G NRZ for cost and power optimized point designs
- Even within common modulation, there will be multiple SerDes variants to optimize power and cost
- Multi-rate SerDes (ex: 10/25/50) will be required to support multiple applications
- Increased complexity for Designers, Test & Measurement, and CAD suppliers
- The days of Model T and any color as long as it is black are over

50Gb/s Electrical I/O Design Considerations

Thank you

