Developments at Finisar AOC

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ABSTRACT

In 2007 Finisar completed the transfer of an entire epi and fab line from one facility to another. During this period, reliability models had to be re-validated and product continuity maintained. In this paper we describe the activities necessary to support such a transition, and we extend previously published VCSEL failure atlases.

Keywords: VCSEL, vertical cavity surface emitting laser, reliability

1. INTRODUCTION

2007 was a momentous year for vertical cavity surface emitting lasers (VCSELs). For the first time, as many VCSELs were shipped outside the data communications market as inside.1 And Finisar’s Advanced Optical Components Division (AOC), perennially the world’s largest-volume VCSEL supplier, completed a facility move that began in 2005. While the linear distance was only ten miles, relocation of the entire epitaxial growth, wafer fabrication, and assembly factories was in many ways more difficult than starting a brand new company. Unlike a startup without existing customers, Finisar had to manage the move in a way that did not jeopardize ongoing volume supply, and to not just meet industry standards, but also to match prior parametric distributions—a much more difficult proposition. All of this had to occur without any reduction in the reliability for which Finisar was famous, and that reliability continuity required proof, proof that could take months or even years to establish because the products from the original facility were already so reliable. Adding to the difficulty was the fact that each customer had different ideas of what constituted acceptable evidence, and each was sensitive to different product characteristics, so multiple types of testing were required, and the old facility could not be shut down until the last customer was satisfied.

This paper will largely be concerned with VCSEL failures. It is important to be clear at the outset that this concentration is not because so many failures occur; Finisar reliability metrics have a stellar history and continued to improve during 2007, and reliability testing for new products again showed improvement over their predecessors. Rather the seemingly inordinate preoccupation with the few failures that do occur and the concentrated effort to understand their causes is precisely what leads to the excellent reliability for which Finisar products are reputed. Relentless, even obsessive, failure analysis is the basis of failure elimination.

Finisar has for several years published internal and external metrics of AOC VCSEL reliability, demonstrating a continuing improvement trajectory even as reported failures approach an almost unmeasurable 1 ppm. Figure 1 shows those metrics updated to include 2007.

![](image-url)

Figure 1. Progress of internal (left) and external (right) measures of Finisar AOC VCSEL reliability.
The internal measure is based on sample reliability testing of production components, with more than a million components included in the samples. The external measure is based on confirmed failures of shipped assemblies. Even with “seven-digits” annual shipments, the less than 2 ppm failure rate for 2007 leads to a small number of failures available for analysis, but analysis of that small number leads to even smaller numbers in the future.

2. RELIABILITY MODEL UPDATE

As improved process controls or new designs lead to improvements in reliability performance AOC periodically publishes updated reliability models. Because the data to support model updates typically takes at least a year of testing, and must include time to actual failure even in the lower stress test groups, model updates become progressively more difficult to provide as reliability improves. In 2007 we introduced a modified epitaxial design targeting improved overall performance in 8 and 10 GBPS applications. Reliability testing for this design began in 2006 and continues to the present, because low-stress groups do not yet have any failures.

The testing for new or modified designs must characterize reliability over the entire range of possible operating conditions, so it generally includes many different temperatures and currents. In this case, there were six ambient temperatures ranging from -40°C to +150°C, and five different currents ranging from 6 mA to 20 mA, thirteen separate test groups in all. As noted, most of the lower stress groups have no failures to date, so it is impossible to establish a reliability model with high confidence, but the failures that have occurred in the highest stress groups allow establishment of a lower bound. Figure 2 compares the reliability of the new VCSEL design to that of the earlier 10 GBPS generation. All stress conditions are accelerated to a single standard comparison condition. The dotted line shows the lower bound estimate is at least a factor of two improvement, but the actual cumulative failure points (diamonds in the figure) range from a factor of two to a factor of ten.

3. MOVE QUALIFICATION

The move of Finisar’s VCSEL manufacturing operations spanned two years, 2005 to 2007. The manufacturing processes moved included epitaxy, wafer fabrication, TO component assembly and test, OSA component assembly and test, plus all supporting operations like shipping and engineering. The move was closely coordinated with customers and with supporting reliability verification qualifications.

For assembly processes relocation was qualified through statistical comparison of key process results (ESD, die attach, wire bond, can weld, test) for the old versus new locations, along with reliability verification of a typical TO+OSA product for the overall manufacturing process (temperature cycling, temperature-humidity bias, high temperature operating life).

The epitaxy and wafer fabrication move entailed establishing two complete process lines, one at the old location and one at the new, and running the two lines in parallel until the last product qualification was accepted. Each processing tool was qualified for each process, and then each device type was qualified with the overall epi/fab process. More than ten VCSEL and photodiode device types were qualified with characterization, mechanical tests, and high temperature operating life, where acceptance criteria included statistical comparisons of the same product from the two locations. Typical test plans and an example reliability comparison appear in figures 3 and 4. For many products multiple customer qualifications were performed using TO/OSA assemblies. Transition of shipments from old to new epi/fab location material was complete by mid-2007, after which the old location epi/fab equipment was shut down and moved.
to the new location. The net result is approximately double the fabrication capacity and further improved line up-time enabled by tool redundancy.

4. ESD IN SINGLE MODE VCSELS

ESD damage has long been known to be one of the most important causes of VCSEL failure. A fairly complete atlas of damage due to ESD has been compiled, showing the locations and features of damage associated with various types of ESD exposure, but most of the previously published atlas has concentrated on multi-mode VCSELS of the sort intended for data communications applications up to 4 Gbps. These VCSELS typically have current apertures of 10 µm or greater diameter, and generally have series resistances well below 50 ohms. Single mode VCSELS typically have smaller apertures and larger series resistance, and consequently

![Figure 3. Typical device move qualification testing.](image-url)

![Figure 4. Example reliability comparison test.](image-url)

![Figure 5. Single mode VCSEL before (solid) and after (dotted) ESD exposure emitted power and reverse current curves for forward and reverse polarity ESD pulses.](image-url)
have substantially lower ESD damage thresholds.\textsuperscript{4} As multi-mode data communications moves to higher data rates, the typical VCSEL aperture is necessarily shrinking, making these devices more like traditional single mode VCSELs in their ESD tolerance, with the added disadvantage that no ESD protection structure can be added since these high speed applications disallow the added capacitance that attends such structures.

Simulations of HBM (human body model) ESD events in typical multimode VCSEL structures typically show that current crowding near the edge of the oxide aperture leads to maximum temperature rise within a micrometer or two of the oxide edge, as verified by TEM (transmission electron microscope) images of ESD-degraded parts, so damaged regions typically form a halo around the edge of the device.\textsuperscript{2,5} In a single mode VCSEL, however, with their much smaller apertures, two micrometers from an edge may well be past the center of the aperture, so we would predict that damage would occur near the center. In addition, the higher series resistance means that a greater fraction of the total power dissipation during any ESD event is due to $I^2R$ heating, which occurs in the mirrors, not in the junction plane. While HBM ESD in multimode VCSELs almost invariably causes damage that transects the junction regardless of polarity, in single mode parts it is possible for forward-bias ESD pulses to cause sensible damage to mirror only, with no active region effect. As a result, while reverse-bias HBM pulses invariably damage the junction, as revealed by increased reverse leakage current and degraded threshold current, Figure 5 shows it is possible for forward-bias HBM pulses to affect only the slope efficiency, by degrading the mirror transmission. These curves are typical of multiple parts intentionally subjected to damaging forward or reverse biased ESD pulses.

TEM signatures of single mode VCSEL degradation by ESD are also different from those previously presented for multi-mode VCSELs, as can be seen in Figure 6.

![Typical reverse-bias HBM damage immediately after ESD exposure. Damage zone is always off-center in direction of maximum contact area (see left).](image)

![Typical forward-bias HBM damage after ESD exposure and extended burn-in. Dislocation array propagates if initial ESD damage reaches active region.](image)

Figure 6. TEM views of HBM ESD damage to single mode VCSELs. Signatures are typical of images from several parts of each type.
Forward biased HBM ESD pulses that caused any damage at all invariably caused damage to the mirror layers surrounding the oxide, but often did not cause damage reaching the quantum wells, and the degradation in current-power characteristics could be relatively small, often degrading power at a fixed current by less than 10%. Extended burn-in and other environmental testing of several hundred parts exposed to damaging forward bias pulses indicates that most have reliability similar to that of parts never exposed to ESD. For damaging reverse bias pulses, however, every damaged part showed severe damage, and subsequent burn-in invariably led to rapid propagation of dislocations across the active region.

We have also performed CDM (charged device model) ESD testing on our single mode parts, finding surprisingly high damage thresholds. Damage did not occur in either forward or reverse bias testing until at least 1500 V was applied, and when damage did occur it invariably was so severe it was evident in vaporized metal and semiconductor on the device surface. An example appears in Figure 7. Subsequent burn-in tests demonstrated that there was no latent damage associated with CDM events: either there was dramatic degradation immediately after the ESD pulse, or reliability was the same as if no ESD exposure had occurred.

5. 2.5 PPM: THE LARGEST SINGLE FAILURE CATEGORY IN 2005

In 2004 and earlier years, ESD dominated VCSEL field failure rates, accounting for nearly 75% of all failures, and effectively masking other failure causes.2 AOC and their customers expended significant effort to improve processes and within two years saw ESD-related failures decrease to the point that they are no longer in the top three causes of field failure. Near-elimination of ESD is a significant contributor to the more than five-fold improvement in field failure rate from 2003 to 2007. But now those other causes of failure, previously dwarfed, become the tallest bars in the Pareto chart. In 2005, the largest single failure cause—at less than 3 ppm!—was stacking faults.

As planar defects, stacking faults occur in crystals due to the passage of a partial or “imperfect” dislocation whereby the normal stacking sequence of close-packed planes is disrupted within a portion of the crystal (a more complete description of stacking faults in VCSELs can be found in reference 6). In contrast, passage of a perfect dislocation maintains the normal stacking sequence such that the extent of the lattice disruption is confined to the linear dislocation itself.7,8 Once generated, these linear features can extend a significant distance from the point of origin, as shown in TEM cross section in Figure 8, where several stacking faults extend completely across all of the VCSEL layers and off the image into the substrate. Stacking faults are generally invisible from the wafer surface, but appropriately filtered IR microscopy reveals them as the faint lines evident in Figure 9.

While stacking fault creation is possible during epitaxial growth, due for example to growth around a contaminant, it is also possible to generate stacking faults by application of sufficient mechanical force to the completed VCSEL. It turns out to be quite difficult to generate stacking faults intentionally, however. The 2006-07 investigation into what had been the largest failure cause for the two prior years ultimately involved almost every source of mechanical trauma imaginable, but VCSELs are remarkably tough creatures. An abbreviated list of the stressors employed in an attempt to produce stacking faults includes intentionally misaligned and damaged saw blades, thermal cycling from cryogenic to highly elevated temperatures, repeated exposure of cantilevered wafers to rapid thermal anneal at temperatures 100°C above the normal process, compression of 320 grit abrasive particles against the wafer surface as well as , and extreme electrical overstress. In addition, hundreds of thousands of dice were inspected for
stacking faults at the wafer level, and retains from shipped wafers were checked. With the few exceptions described later, no stacking faults were ever found.

Several of the mechanical and thermo-mechanical stress conditions caused macroscopic damage such as extensive mechanical cracks. These could always be distinguished from stacking faults, either by lack of linearity or by orientation (the stacking faults always follow the \{111\} direction). Ultimately, stacking faults were produced by only two of the stressors attempted: extreme electrical overstress and extreme mechanical point stress applied to the VCSEL surface. In both cases, the stress level necessary to induce stacking faults was also sufficient to cause other, more evident damage. Nevertheless, these two causes, illustrated in Figure 10, provided guidance on aspects of the process where increased vigilance was warranted, and the investigation engendered tools that make ongoing detection and elimination of of stacking faults possible.

Knowing the types of processes that might cause stacking faults was an important step. While with very low defect rates it is never certain which of several corrective actions is primarily responsible for their eradication, in this case the effects are evident in the field results. As shown in Figure 11, stacking faults fell from the largest single field failure cause in 2005 to an almost undetectable 0.2 ppm in 2006, and were zero in 2007.

6. ARRAY RELIABILITY

Since the relative ease of fabricating even very large arrays of emitters is one of the significant advantages of VCSELs, but when failure is defined as degradation of any single element in an array a chip with multiple emitters necessarily has

Figure 9. Filtered IR image of energized VCSEL with stacking faults.

Figure 10. The only two stressors found to produce stacking faults in fabricated VCSELs.

Figure 11. Stacking faults, the largest single cause of field failures in 2005, eliminated by 2007.
reduced reliability, the question of just how reliability scales with element count is an important one. (Of course, if the system architecture is forgiving of a small number of degraded elements in an array, a large array could actually have higher reliability than a single element, but this architectural solution is often not a design option.) A recent review has realistically assessed the effects of both wearout and random failures on array reliability, reasonably speculating that some correlation of degradation rates for proximate elements might make estimates of array reliability scaled from single element statistics unnecessarily conservative.\textsuperscript{10} Using the STABILAZE\textsuperscript{\textregistered} process, which allows simultaneous burn-in of all elements on an entire wafer, and subsequently probing those all of those elements, we have been able to demonstrate just how some of these proximity correlations occur, verifying the speculation.

Using the STABILAZE wafer level burn-in process, wafers were first subjected to the short burn-in intended to stabilize their performance prior to probe. After probing established the characteristics that would have been present if dice were accepted for shipment, the wafer was subjected to a longer wafer level burn-in, one simulating more than five years of typical system operation. Figure 12 shows that the degradation experienced during this extended burn-in is variable across the wafer, but that the greatest degradation clusters in relatively small regions of the wafer. Presumably, if arrays of VCSELs were selected from these regions there would be a higher probability of multiple elements on the array failing, which also means that arrays selected from other regions of the wafer would have fewer failures. If array failure is defined as failure of one or more elements, the aggregate failure rate for arrays would be less than the failure rate predicted from single element data.

The preceding test is relevant for prediction of failure rate due to wearout. While wearout is more of an issue for arrays because of the higher total power dissipation and thus somewhat higher operating temperatures, and though wearout is almost always what dominates twenty-year life even for single elements, for most applications the more relevant question has to do with the random failure rate, which typically dominates during at least the first few years of life. For arrays this is even more true, because unless failures are correlated by area the array failure rate increases linearly for random failures, but at a much lower rate for wearout failures. This is a consequence of the typically lognormal distribution of wearout failures, and it means that if the random failure rate is high that large element-count arrays will be impractically unreliable. We can use the same STABILAZE process to evaluate the random failure area distribution for Finisar VCSELs, though unlike the wearout area distribution in Figure 12, which can reasonably be extrapolated to the production devices, random failures generally have individual causes and might be removed by processes subsequent to the wafer level burn-in. In particular, the automated visual inspection after saw, which removes chips with damage or epitaxial defects, will decrease the incidence of causes of random failure (that this is certainly the case is evident in the field failure statistics cited above). Nevertheless, it is reasonable to investigate whether random failures exhibit clustering across the wafer. If they do, they are likely to do so in the array chips from that wafer, making predictions from single element results even more conservative. Figure 13 shows two views of the same wafer for which gradual degradation was presented in Figure 12. Each black dot represents a single element that degraded at least 2 dB during the extended wafer level burn-in. In the view on the right, it is evident that even in the absence of subsequent screening processes very few (<0.1%) of the elements that passed normal probe limits at the beginning of burn-in might subsequently degrade. More importantly, however, if one looks at all elements, including those that would never have passed probe parametric limits, let alone the subsequent inspections, there is clear clustering of degradation, especially near the upper left.
While these tests validate the speculation that array reliability is better than might be extrapolated from single element data, they do not allow exact calculation of just how conservative those single element extrapolations might be. Even if there were no area correlation, however, a reasonable bound on one-year failure rate could be computed from the single element field failure rate described above. Using those figures, and the definition that a single failing element fails an entire array, a four element array would have one year failure rate of 8 ppm, and a twelve element array would have 24 ppm. These are quite respectable numbers, similar to the failure rates for single elements only four years ago.

7. CONCLUSIONS

Finisar field failures from all causes continued to decline during 2007, even as a new facility came fully on line. In large part this was due to a continuing obsession with failure identification and eradication. Such an obsession is required if improvement is to continue as failure rates for existing designs approach 1 ppm. As new applications require smaller active regions with higher current densities, new design approaches are also necessary, because otherwise wearout reliability cannot keep pace with the reduction in random failures.

In the mid-1990s it was VCSEL reliability that made possible the current industry of VCSEL products, first in data communications, and now in an expanding range of other applications. While VCSELs have many other desirable attributes, it seems certain that reliability will figure importantly in their future, as it has in their past.

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REFERENCES