Datacenter Bottleneck Solutions & Crystal Ball for Panelists

How Can Optics Address Bandwidth and Latency Bottlenecks in Data Centers?

OMIF OFC Workshop

Anaheim, California

18 March 2013

Chris Cole

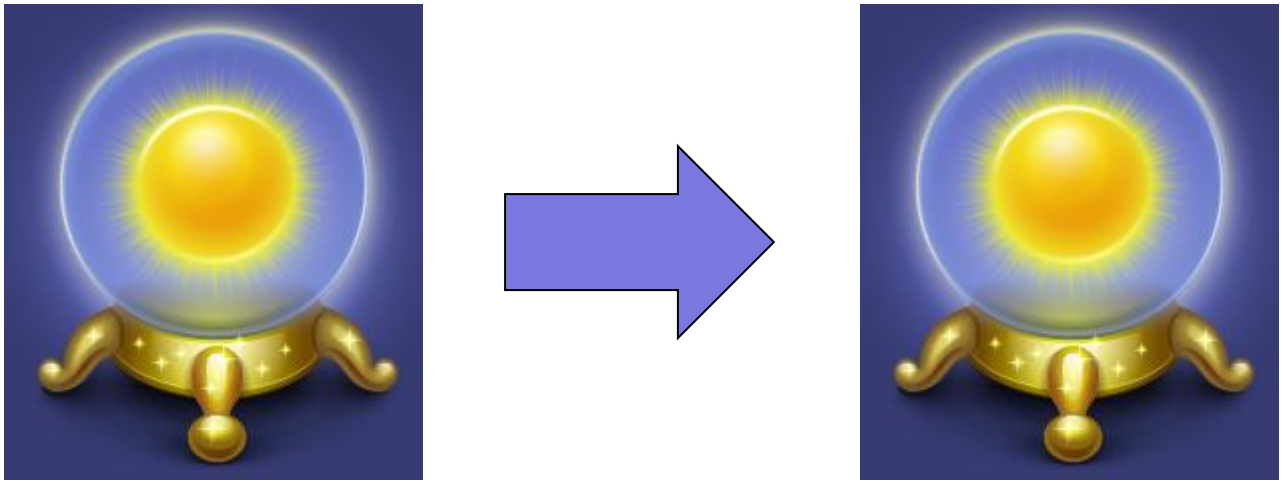
OFCNFOEC 2013

THE FUTURE OF OPTICAL COMMUNICATIONS IS HERE

Finisar®

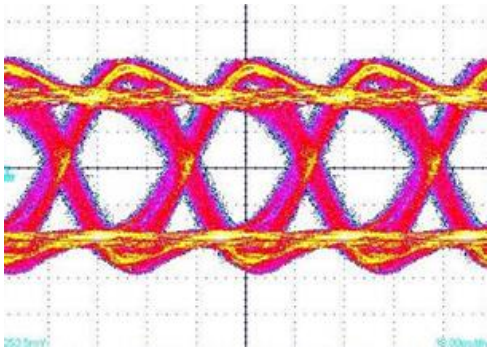
Higher Lane Rate

Ashok Krishnamoorthy (Oracle)



40G low-power Server I/O

- MMF AOC
- 40Gb/s Serial VCSEL eye

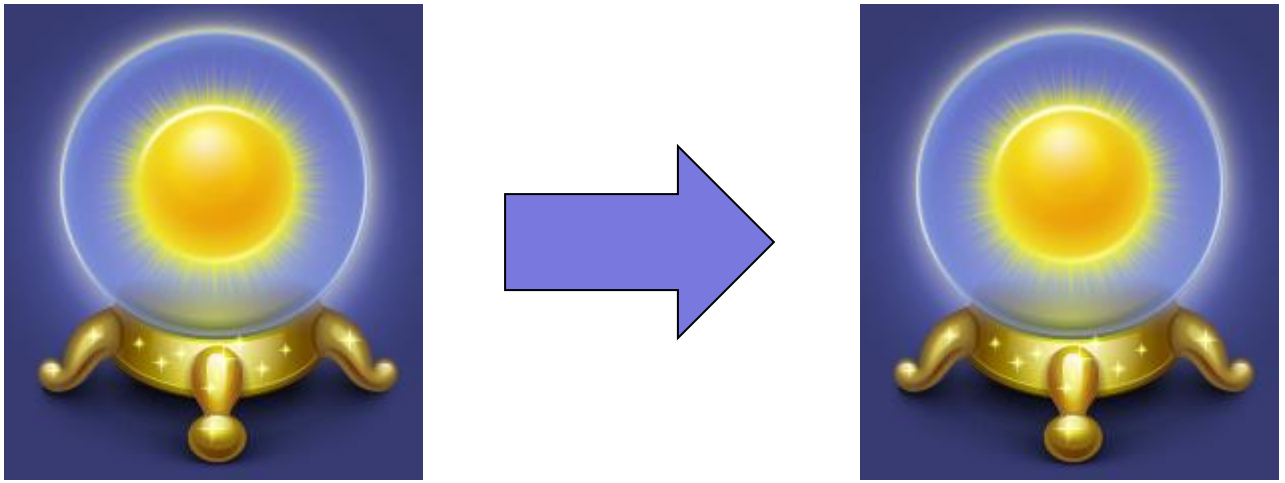


100G low-power Server I/O

- MMF AOC
- 2x 50Gb/s
- OFC'13 IBM/Finisar paper on 56.1Gb/s VCSEL link (OW1B.5)

Higher Link Rate

Marc Cohn (Ciena)



400GbE

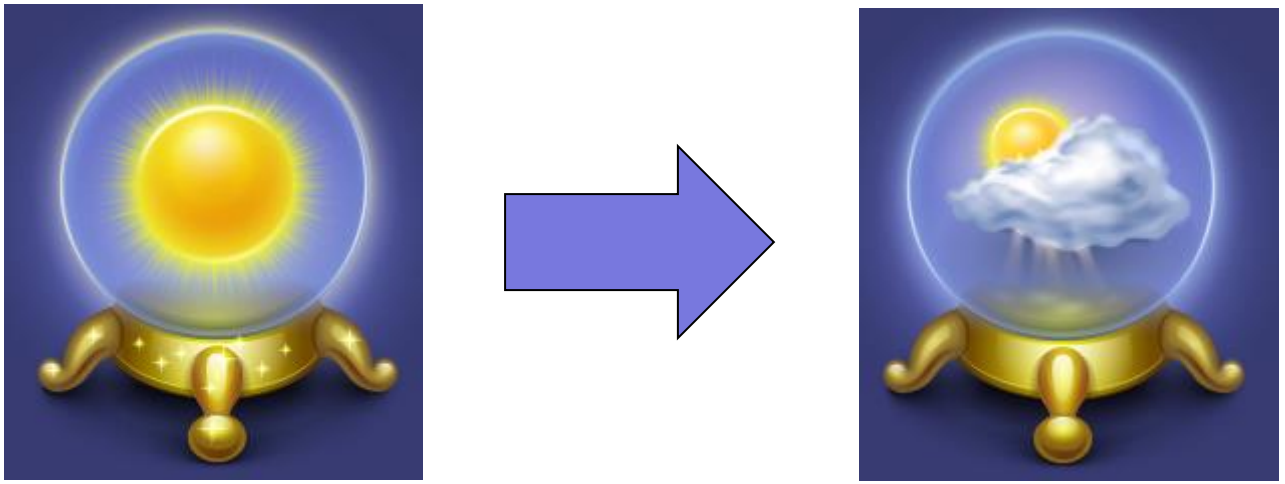
- Mar'13 proposal to IEEE
- MAC/PCS focus
- Possible Gen1 PMDs: 16x25G NRZ

1.6TbE

- Next likely Ethernet rate
- Will require fundamentally new technology

Parallel MMF

Mitch Fields (Avago)



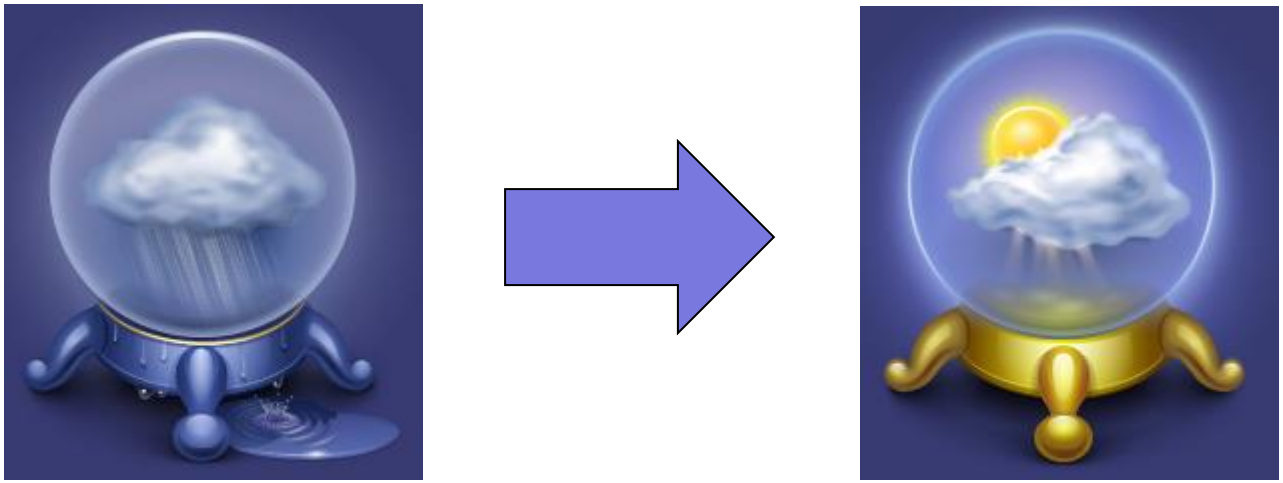
VCSEL Arrays:

- 4x10G (40GbE-SR4)
- 10x10G (100GbE-SR10)
- 4x25G (100GbE-SR4)
- 12x25G (OE)
- 1x12, 2x12 MPO connectors

- 24x25G Finisar OE at OFC
- 16x25G (400GbE-SR16)
- 2x16 MPO connector

WDM

Mehdi Asghari (Kotura)



C-band (~1550nm) Si chips

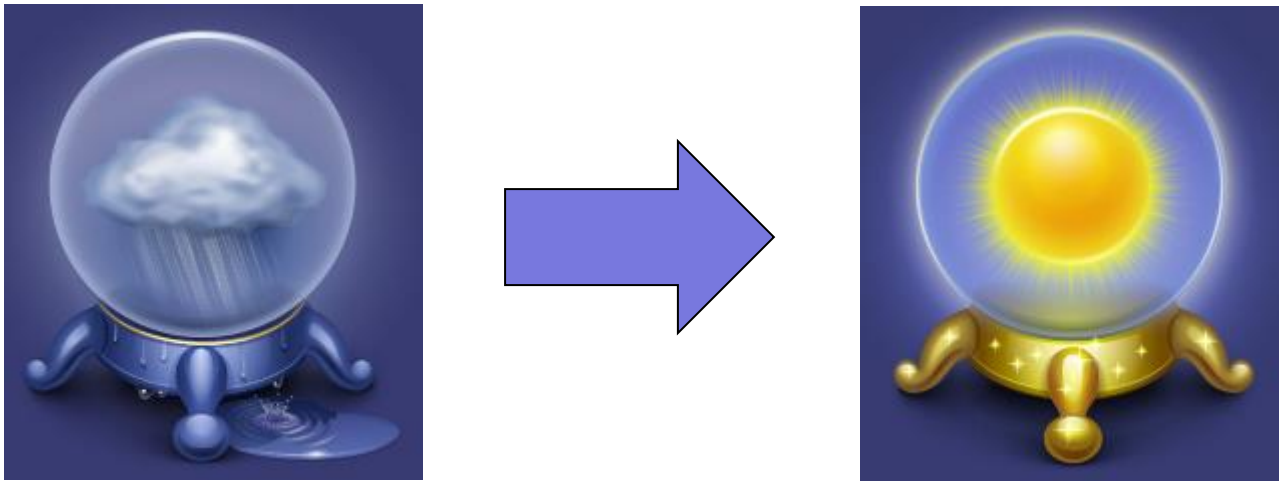
- Proposed for IEEE 100G
- Jan'13 Straw Poll #1:
  1 out of 97 voted in support of C-band
- Unlikely in the datacenter

Switch to O-band (~1310nm)

- Standard wavelength(s) for datacenters (LR, LR4)
- Used by all other IEEE 100G SMF PMD proposals
- Major process change ☹

WDM

Marc Taubenblatt (IBM)



CWDM (20nm $\Delta\lambda$) Si chips

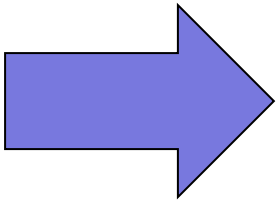
- Proposed for IEEE 100G
- Minor cost savings over LR4 w/ similar packaging
- 60nm too wide for many Silicon (Si) techniques (ex. grating coupler)

Develop 100GbE-LR4 WDM (5nm $\Delta\lambda$) Si chips

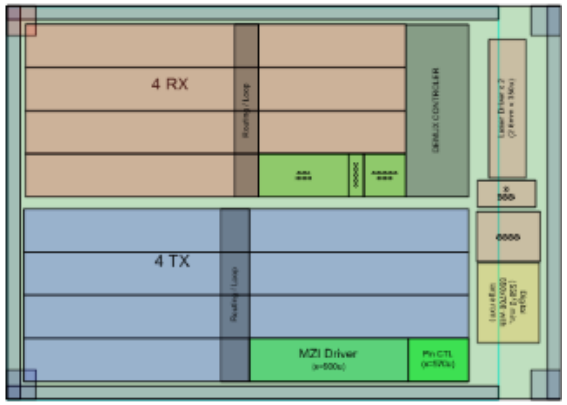
- 15nm compatible with all monolithic Si and InP techniques
- Interoperable with installed 100GbE-LR4 base

WDM

Peter De Dobbelaere (Luxtera)



100GbE-LR4 WDM Si chip



- Presented by Brian Welch at IEEE Jan'13 meeting
- LR4 Si QSFP28 cost = **3.5x** SR10 CXP cost
- Peter will retire after billion dollar acquisition

Parallel SMF (PSM)

Tom Issenhuth (Microsoft)

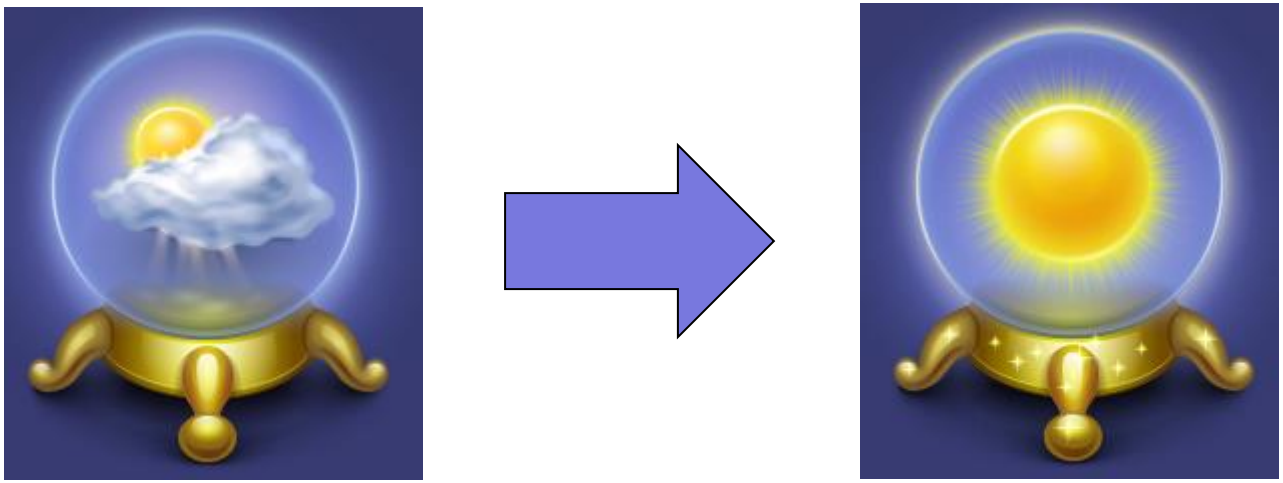
All SMF datacenter

- PSM4:
  4x 10G/fiber, 4x 25G/fiber
- Link total cost higher than
  SMF WDM for >300m &
  MMF parallel for <100m
- Lower OpEx?


Rapid
A fatal exception 0E has occurred at 0028:C0011E36 in VXD VMM(01) +
00010E36. The current application will be terminated.
* Press any key to terminate the current application.
* Press CTRL+ALT+DEL again to restart your computer. You will
lose any unsaved information in all applications.
Press any key to continue _

Parallel SMF (PSM)

Tom Issenhuth (Microsoft)

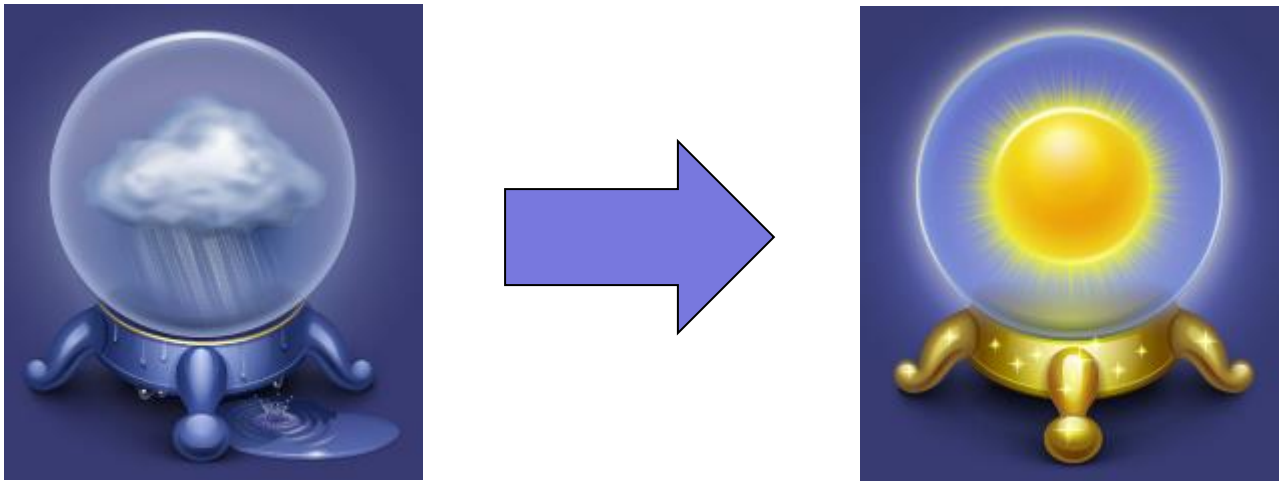


All SMF datacenter

- PSM4:
  4x 10G/fiber, 4x 25G/fiber
- Link total cost higher than WDM SMF for >300m & Parallel MMF for <100m)
- Lower OpEx?
- 2x50G/fiber
- Multi-core fiber
- WDM (ex. LR4):
  1x 40G/fiber, 1x 100G/fiber
  4x fiber plant capacity
- Parallel + WDM

Higher Order Modulation (HOM)

Adam Carter (Cisco)

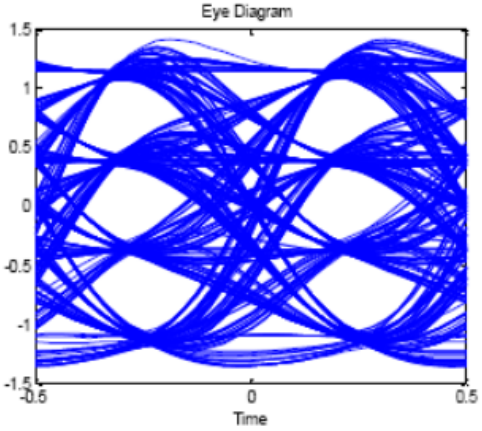


PAM-8 44Gbaud (& PAM-16)

- Proposed for IEEE 100G
- Impractical because of:
  - Excessive SNR
  - Stringent Laser RIN
  - Stringent MPI

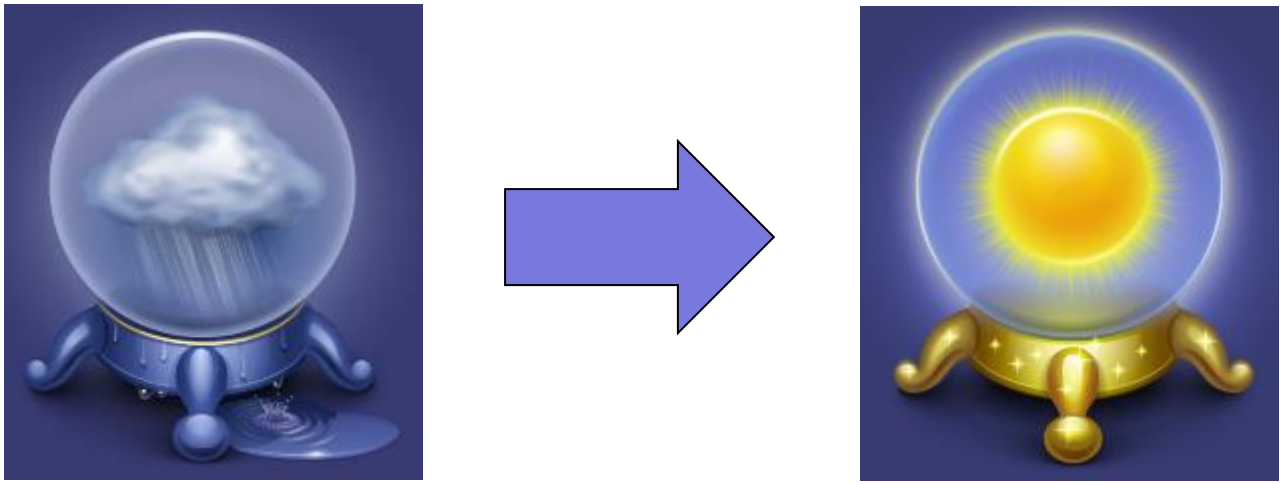
PAM-4 50GBaud

- Practical in time frame of 50G I/O
- or QAM
- or DMT

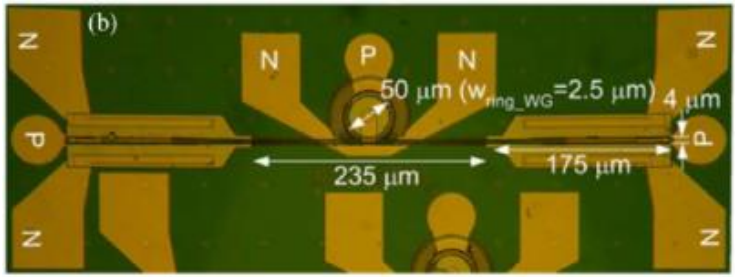


Silicon Photonics

Andy Bechtolsheim (Arista)



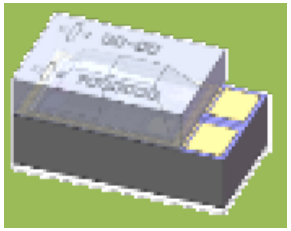
Hybrid Silicon Laser (UCSB)



- Years until volume commercial production

- 4x25G VCSELs

- or packaged laser source for Si (ex. Luxtera)



Multi-Channel Pluggable Modules

Chris Cole (Finisar)

Ex. 400GbE-LR4 CFP2

- 8x50G I/O
- duplex LC
- WDM HOM
- 10 ports
- 4Tb/s line card

Multi-channel MLG CFP2s

- 8x50G I/O (same slot)
- MPO
- 4x 100GbE (40 ports)
- 10x 40GbE (100 ports)
- 32x 10GbE (320 ports)

Datacenter Bandwidth Bottleneck Solutions

Traditional

- Higher lane rate: 40G, 50G
- Higher link rate: 400GbE, 1.6TbE
- Parallel MMF: 2x, 4x, 12x, 16x, 24x
- WDM

New

- Parallel SMF: 2x, 4x, multi-core fiber
- Higher Order Modulation: PAM-4, or QAM, or DMT
- Multi-channel modules (MPO, MLG): 10, 40, 100GbE

Characteristics

- Material systems: GaAs, InP, Si
- No magic bullet & no free lunch
- Innovation in many areas