High power VCSEL arrays for consumer electronics

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ABSTRACT

Finisar has developed a line of high power, high efficiency VCSEL arrays. They are fabricated at 860nm as traditional P side up top emitting devices, leveraging Finisar’s existing VCSEL fab and test processes for low cost, high volume capability. A thermal camera is used to accurately measure temperature profiles across the arrays at a variety of operating conditions and further allowing development of a full reliability model. The arrays are shown to demonstrate wear out reliability suitable for a wide range of applications. Typical $1/e^2$ beam divergence is near 16 degrees under CW operating conditions at peak wall plug efficiency, narrowing further under pulsed drive conditions.

Keywords: VCSEL, array, thermal, high power, reliability

1. INTRODUCTION

Finisar is introducing a range of high power VCSEL array products to meet customer demand across a range of high volume low cost applications. These devices use the same production facilities in Allen Texas, and established fabrication processes already implemented in Finisar’s line of communication VCSELs. Key features, in comparison to more aggressive high power VCSEL technologies, include P-side up emission, and implementation of conventional die thinning processes, instead of substrate removal by wet etch.

Because of its synergy of low cost per unit area, damp heat survivability, usable beam quality, and the infinite configurability of array layout, high power VCSEL array technology is experiencing significant demand across a wide range of application spaces. But almost every application is customer specific and can require different design tradeoffs for wall plug efficiency, cost, beam divergence, power, and uniformity. These designs do seem to fall into three different general classes, which are described below. The subject of this work is to describe the general methodology we are developing for reliability test and qualification across these different product classes, and to show some of the pitfalls encountered along the way.

DC Illumination

![Die photos, power levels at peak conversion efficiency, and emitter count for 3 array sizes of high power array die for DC illumination applications.](image)

These die, shown in figure 1, are intended to replace LEDs in applications where pulsed operation is not desired, such as security cameras and some set top boxes. Because VCSELs have much higher brightness than LEDs they can illuminate a narrow field of view with much greater electrical efficiency, thus allowing a much smaller camera/array illuminator footprint. These arrays must be attached to an adequate heat sink, and are rated to maintain their efficiency and power up to 50°C. For this array class, Finisar currently uses a nominal emitter pitch of 50 microns to limit self heating and an
oxide aperture diameter range of 12-14 microns. Typical power output for a 1W (at peak efficiency greater than 40%) design is shown below in figure 2. Note the design shown is generally capable of more than 1W output and higher temperature operation, but with de-rated reliability and wall plug efficiency. The first variant of this design that Finisar has fabricated and is performing reliability test development on has a nominal wavelength of 860nm.

Figure 2. Power output versus current and relative wall plug efficiency for 0.75mm² DC high power VCSEL array. Curves shown for 12 and 14 micron apertures.

**Quasi-CW and reduced duty cycle**

A second class of high power array implementations is forming around reduced duty cycle operation. Applications include gesture recognition, based on time of flight and array imaging techniques for 3 dimensional machine vision. In these applications optical output can be synchronized with a camera so that constant power operation is not needed, and often not desired in order to allow acceptable eye safety levels. Overall duty cycles in this application range are on the order of 5-20% and compared to CW designs much higher peak power levels are possible. In this regime of operation, the maximum peak power that can be achieved before rollover is a strong function of the pulse width used.

Figure 3. Peak output power and relative efficiency at 50°C, 10% duty cycle operation for a 0.75mm² high power die with 384 12um aperture emitters in a hex pack pattern. Pulse widths ranging from 200ns to 10ms are shown.
Figure 3 shows light versus current operation over pulse width ranging from 200ns up through 10ms. This range of pulse widths spans both the thermal time constant of single heating VCSEL (nominally ~1us) and the time required for mutual heating effects to occur in a VCSEL array (1-2ms). For pulse widths over 10ms, little additional peak power above CW levels can be achieved. In this application space, a range of oxide apertures and custom emitter layouts are often used depending on customer requirements for pattern, divergence, efficiency, and power density, but overall emitter densities can be higher than in constant power applications.

**Low duty cycle, pulsed**

This operation mode is intended for applications such as automotive LIDAR and range finding. Pulse widths are of 1us or less and are used at very low duty cycle, typically less than 1% to achieve high peak power levels. Much larger VCSEL apertures can be used to maximize peak power as heating effects that drive optical index changes across the oxide aperture have not had time to occur. In this mode, the arrays are operated well beyond peak wall plug efficiency. Relevant specifications include operating voltage, peak power, and divergence. Figure 4 shows peak power output for a range of prototype large oxide aperture arrays, all arrays shown use the same standard 0.75um² area die footprint and come from the same wafer. Power levels of >35W can be reached at 70°C. Highest peak power was achieved using 26µm emitters at maximum density. These were the largest prototype array apertures tested.

![Figure 4. Peak power and wall plug efficiency shown over temperature for multiple 0.75mm² array layouts. Best power output shown for 26um apertures on 50um pitch. Data is shown over temperature for 500ns pulse width at 0.5% duty cycle.](image)

**2. HIGH POWER VCSEL ARRAY RELIABILITY**

Determining array reliability using accelerated aging tests presents unique challenges in comparison to the usual datacom single emitter work. The high power dissipation of array devices and the resulting temperature gradients both across the array and across reliability test equipment itself, especially under the accelerated conditions usually used in such testing, can lead to failure modes different from the wear out processes under evaluation. Finisar is developing a general methodology for high power array reliability evaluation that leverages well understood single device behavior and further uses a high-resolution infrared camera and microscope along with re-engineered reliability test equipment to provide accurate high power array reliability models. These methods, along with results for our DC illumination devices, are presented in this section.
Single element reliability

For determination of expected life during use in singlet datacom devices, the modified Arrhenius acceleration model is used. Work describing the implementation of this model on datacom VCSELs with InGaAs quantum wells, similar to the wells in our power devices, has been published elsewhere [1,2]. The work was performed in the development of 14 and 28 Gbps datacom VCSELs using relatively large sample sizes and over many temperature/current combinations and variations in design, allowing development of reliability models with relatively tight confidence bounds. Effective implementation of an Arrhenius model requires an accurate description of junction temperature, which can be derived from measurement of wavelength shift of the lowest order mode in single emitters. Typical wavelength shift in these VCSELs over temperature is near 0.065nm/C. For 860nm InGaAs quantum well VCSELs, as well as VCSELs at longer wavelengths with higher indium levels, Arrhenius model [3,4] activation energies around 1.3-1.5eV are typical compared to 0.7-0.8 eV for GaAs quantum well devices. Current acceleration exponents are typically 3-5. The high activation energy of InGaAs VCSELs can lead to very long expected wear out times, over 1000 years, under normal use conditions (~50°C) in single emitter applications, but the expected life drops rapidly with increasing current and temperature, as shown in figure 5.

![Figure 5. Plots showing time to 1% failure for InGaAs single VSCELs versus temperature and drive current.](image)

Thermal imaging of single VCSELs and arrays

High resolution InSb based thermal cameras with fast frame integration times, as low as 0.5ms, have become available in recent years. Wavelength sensitivity of these cameras is in the 3-7 micron range. When equipped with an IR microscope objective, they can allow infrared imaging with a nominal resolution of about 3 microns, and temperature determination on the same length scale when appropriate corrections are used. Figure 6 shows an IR image for a series of single VCSEL emitters of varying oxide aperture diameter on a single chip. Only the device on the far left is biased at 12mA. The other devices in the picture are unbiased. Aperture regions are clearly visible, as are the very low emissivity gold contacts. By measuring thermal camera based temperatures and optical emission spectra across many single VCSEL aperture diameters, temperatures and drive currents, we are able to construct a good fit model for VCSEL junction temperature using only oxide aperture and thermal camera apparent temperature as inputs. This model can then be used to image VCSEL junction temperature across arrays constructed on the same epitaxial material and under various drive conditions.

![Figure 6. IR microscope image showing single biased VCSEL on left, three unbiased devices to the right. Other VCSEL features such as contact metal and apertures are visible due to differences in material emissivity.](image)
Figure 7 shows a sample IR microscope image of a 2W, 383 element DC high power array operating at 4A DC bias at 50°C substrate temperature, with a junction temperature profile for devices along the line shown in the inset to the right. Peak junction temperature is 115°C or a 65°C rise above ambient. Junction temperature variation across the array at 4A 50°C is approximately 20°C.

Using this methodology, data from a series of many IR array pictures is used in figures 8 and 9 to show peak junction temperature delta above TEC chuck temperature and the junction temperature difference from array edge to the center as a function of drive current per emitter for all 3 high DC high power array designs at multiple TEC chuck temperatures. Notice that for these arrays, peak junction temperature rise increases with both increasing array size and increasing TEC chuck temperature. This can be attributed to the monotonic drop in GaAs/AlGaAs thermal conductivity with increasing temperature. This data and its consequent effects on reliability and VCSEL rollover illustrate the limited scalability of low cost, substrate not removed, high power arrays in DC drive applications. Another important implication of this data lies in the design of reliability test condition matrices for any high power array. Peak junction temperature rise and difference between maximum and minimum junction temperature across the array must be taken into account in order to insure that failure modes other than those desired for the accelerated failure model are not introduced.
Figure 9. Junction temperature delta across each array design, from array center to edge, is plotted as a function of drive current per emitter for TEC (substrate) temperatures of 25, 50, 100, 150°C.

Figure 10. Plot and lognormal fit of failures in time for 2W and 1W arrays taken for multiple test conditions.

Using the junction temperatures derived from IR image data and multiple high temperature test conditions, we are able to construct reliability models for all 3 DC high power arrays. Lognormal plots for two of these arrays are shown in figure 10. For purposes of this model, failure is defined as a 1dB drop in power for the entire array. For the 2W array this data is still rather preliminary with only 113 hours accumulated at the time of writing. But activation energy is 1.3 eV and median life based on peak temperature for the 2W 2.8A, 50°C operating temperature is 69 years, median life based on median array temperature is 621 years. Times to 1% failure for peak and median temperature are 5.7 and 60.9 years, respectively. Note that the difference between peak temperature and median temperature lives means that the center of the array will dim faster than the edges, but the total power available will still be degraded less than 1 dB.
Median life for both the 300mW and 1W arrays are considerably longer, at over 1200 years, with times to 1% failure over 200 years. As noted earlier, the time 1% failure for InGaAs quantum well singlets operating under comparable drive conditions are well over 1000 years, illustrating the profound effects of increased mutual heating on reliability for versions of this array and its intended operating condition.

Figure 11 shows an IR camera image for a much denser QCW array under pulsed drive conditions at a substrate temperature of 75°C. 1 and 10ms pulse widths were used, both at 10% duty cycle, so that both arrays have roughly the same energy dissipation. This prototype device uses 384 emitters 12µm emitters packed in a 36µm pitch hex array. For all of these images, camera integration time is 0.6ms, allowing us to illustrate the onset of mutual heating effects in the array. The first image shows array and temperature profile for 1ms pulse width, maximum junction temperature heating 110°C with a 10°C drop for devices near the edge. The second IR image is for a 10ms pulse, also at 10% duty cycle, image taken at the beginning of the pulse – with 0ms delay. Third image shows strong heating of the array pulse, with a similar image taken at the end of the pulse, after 9ms delay. At that time the image shows a larger 25°C temperature gradient, and a peak temperature almost 75°C above the 75°C substrate.

The strong heating shown in the thermal image of figure 11 is also reflected in the output power distribution of the array. Figure 12 shows a normalized plot where total optical power for each emitter is shown as a color. The same drive conditions are used as in figure 11. In these plots the array is imaged using a precision beam analysis camera, power is integrated for each emitter, and normalized. Power levels and integration times are adjusted so that no emitters in the array saturate the camera. Notice that this particular array has two weak emitters.
For each image in figure 12, the normalized standard deviation of emitter power is calculated across the array and a histogram is shown below the power graphic to illustrate the effects of array heating on array output power uniformity. While these effects may be of little consequence in simple illumination applications, they can be quite relevant for gesture recognition applications where array imaging is required. In general, if uniformity is a critical requirement for an application, keeping drive pulses shorter than the array mutual heating time is critical. This effect is further illustrated in figure 13 below where uniformity is shown to drop to a baseline level once a low enough pulse width is reached, typically less than 100μs.

![Figure 12. Normalized optical output power across the array and associated standard deviation.](image1)

![Figure 13. Normalized standard deviation for power across a custom array showing heating effects for longer pulse widths, substrate temperature, and oxide aperture diameter. Drive condition is 2.5A, 10% duty cycle, pulse widths vary from 1 microsecond to CW operating conditions, shown at 1e7 microseconds.](image2)

### 3. CONCLUSIONS

While VCSEL arrays can scale to quite high powers thermal considerations make reliability assessment significantly more difficult than it is for their single-element cousins. Accelerated tests of large samples can be confused by the large dissipated powers, and even with large heat sinks arrays can heat their neighbors well above the nominal ambient. And across each array the temperature gradient increases significantly as temperature increases. Elevated currents further increase the temperature gradients, and at higher ambient temperatures these effects are more severe, with the final result that different portions of the array age differently, and the array as a whole may age differently—not just faster, but
differently—than it would in normal operation. In this work we demonstrated that a conventional thermal imaging camera, equipped with appropriate optics and properly corrected for offsets between apparent camera temperature and actual junction temperature, provides understanding of these gradients at both nominal operation and under accelerated aging conditions and allows for accurate reliability modeling. The profound dependence of these thermal gradients on ambient temperature, current magnitude, and current pulse conditions makes accurate modeling all the more important. The thermal camera has become an indispensable tool for VCSELs of this sort, where a simple thermometer is just not enough.

REFERENCES