

# Next Generation CFP Modules

Chris Cole

Finisar Corporation, 1389 Moffett Park Drive, Sunnyvale, CA 94089  
Email: chris.cole@finisar.com

**Abstract:** The details of two next generation CFP MSA modules, CFP2 and CFP4 are described. This includes size evolution, front panel port density, electrical I/O, mechanics, MIS, power, and support of SMF and MMF applications.

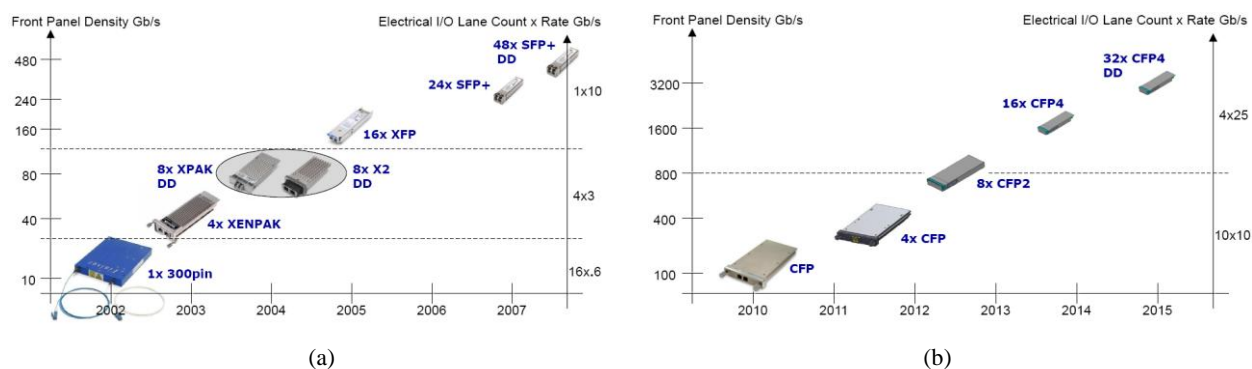
**OCIS codes:** (060.0060) Fiber optics and optical communications; (060.4510) Optical communication; (200.4650) Optical interconnects; (350.4800) Optical standards and testing

## 1. Introduction

The CFP MSA is currently defining two next generation 100G form factors; CFP2 and CFP4 [1], which compared to the existing CFP form factor will double and quadruple front panel port density, respectively. The new form factors take advantage of advances in optics and IC integration, and increase in electrical I/O rate from 10G to 25G. They will support existing and future duplex Single Mode Fiber (SMF) and parallel Multi Mode Fiber (MMF) interfaces.

## 2. Form Factor Evolution

Figure 1 b) shows the evolution of 100G duplex fiber form factors defined by the CFP MSA [1]. Increases in front panel density result from decreases in module size and power. This is enabled by increased integration of optics and ICs, and by increase in electrical I/O rate from 10G to 25G reducing the I/O width from 10 lanes to 4.



**Figure 1:** Historical duplex fiber form factor evolution: a) 10G modules, b) 100G modules.

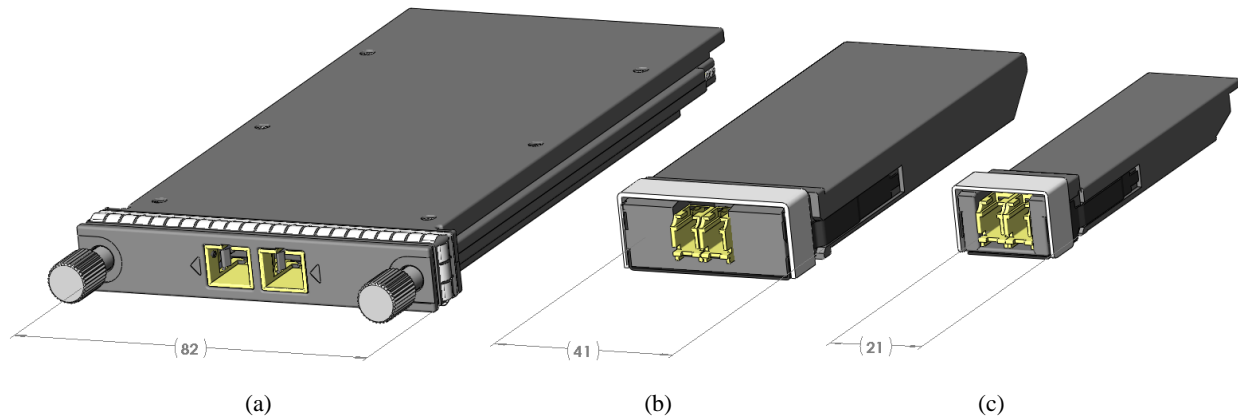
Figure 1 a) shows a similar historical evolution of 10G duplex fiber form factors, enabled through increases in integration and electrical I/O rate. While fewer 10G form factors might have been possible, this would have resulted in delaying front panel density increases by not taking advantage of incremental technology advances. The same motivation of immediately taking advantage of advances in integration and I/O technology drives the CFP form factor evolution to increase front panel density in multiple steps.

## 3. CFP Form Factors

Figure 2 shows drawings of the CFP, CFP2, and CFP4 form factors. CFP modules are shipping today supporting SMF and MMF Ethernet optics defined in the IEEE [2]. CFP2 modules will be introduced in 2012 to double port density, and CFP4 modules will follow a few years later to quadruple port density. CFP2 and CFP4 modules support 4x25G electrical I/O being defined in the Next Generation 100Gb/s Optical Ethernet Study Group [3], which will standardize this interface when it becomes a Task Force. Figure 2 a) shows CFP 360° EMI springs which seal against the front panel opening bezel. CFP2 and CFP4 seal against 360° EMI springs inside the front panel bezel.

## 4. Electrical I/O

CFP has 12x10G TX and RX electrical I/O pairs. CFP2 has 8x25G TX and RX I/O pairs, while CFP4 has 4x25G TX and RX I/O pairs. In addition CFP2 can be reconfigured to support 10x10G TX and RX I/O pairs. All the form factors have an optional reference clock input, as well as optional TX and RX monitor clock outputs.



**Figure 2:** CFP form factor diagrams annotated with faceplate width in mm: a) CFP, b) CFP2, c) CFP4.

### 5. Locking Mechanism

CFP is locked into the host system with two screws which engage the host connector cover, minimizing tolerance stack up between connector plug and receptacle. Because screws take up front panel width, CFP2 and CFP4 are locked in with latch bails similar to other pluggable form factors like XFP and SFP+. The three CFP form factors use the locking action to compress a 360 degree EMI gasket between the module and host connector cover. A similar EMI gasket seals the host connector cover to the host PCBA.

### 6. Management Information System (MIS)

The CFP MIS is made up of two components; the MDIO firmware interface and the hardware control and alarm pins. CFP, CFP2 and CFP4 support the same MIS to enable reuse of host and module firmware. As firmware development and integration becomes the major component of overall optics design, firmware reuse becomes increasingly important.

There are a few minor MIS differences between the three form factors. CFP has five MDIO port address pins which translate into 32 distinct port addresses. This was carried over from XAU1 MDIO definition, and in practice has been found to be unnecessary. The CFP2 and CFP4 MDIO port address pins are reduced to three, allowing up to 8 distinct port addresses. For host cards with more than 8 ports, this requires separate MDIO busses. While CFP2 retains all the CFP programmable alarm and control pins, these are eliminated in CFP4.

### 7. Power

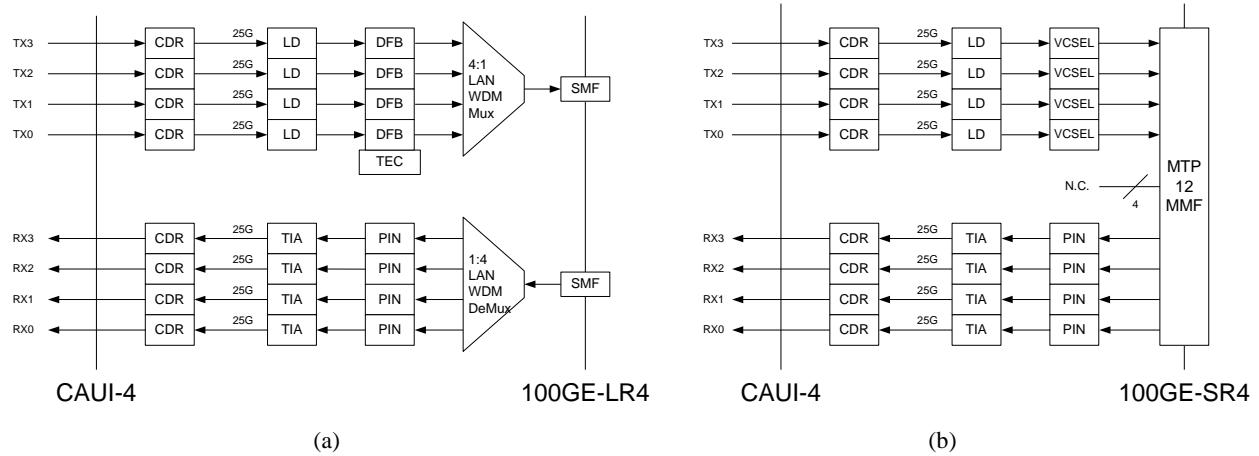
CFP has 20 3.3V power pins, supporting up to 4 power classes with 8, 16, 24, and 32 Watt limits. CFP2 has 8 3.3V power pins, supporting 4 power classes with 3, 6, 9 and 12 Watt limits. CFP4 has 4 3.3V power pins, supporting 4 power classes with 1.5, 3, 4.5, and 6 Watt limits. The lowest power density limit permits operation without a heat sink. The four power limits correspond to progressively higher top surface power densities requiring more advanced cooling techniques. For example, the four CFP4 power densities are 0.7, 1.4, 2.1 and 2.7 Watts/in<sup>2</sup>. CFP4 module dissipating 6 Watts has similar power density and cooling challenges as a QSFP+ module dissipating 3.5 Watts.

### 8. Duplex SMF Applications

CFP2 and CFP4 modules are defined to support existing and future SMF applications. The primary application is 100GE-LR4 10km duplex SMF, as shown in Figure 3a), defined in [2], with CAUI-4 electrical I/O to be defined in [3]. CFP2 will support 100GE-ER4 40km and 100G DWDM optics when integration technology matures. CFP2 and CFP4 can also support the future 100G structured data center 1000m duplex SMF application.

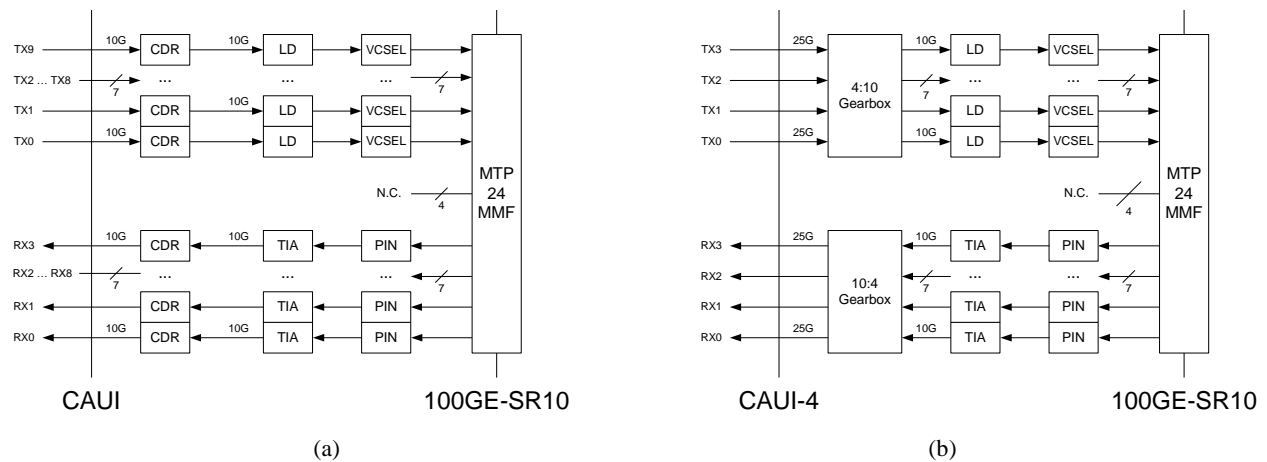
### 9. Parallel MMF Applications

CFP2 and CFP4 modules are defined to support existing and future parallel MMF applications. The primary application is 100GE-SR4 100m on parallel MMF, as shown in Figure 3b), which together with CAUI-4 electrical I/O will be defined in [3].



**Figure 3:** 100Gb/s Ethernet Optics block diagrams: a) 100GE-LR4 duplex SMF with CAUI-4 electrical I/O, b) 100GE-SR4 parallel MMF with CAUI-4 electrical I/O.

CFP and CFP2 modules support 100GE-SR10 parallel MMF with CAUI interface, as shown in Figure 4 a). CFP2 and CFP4 modules can also support 100GE-SR10 with CAUI-4 electrical I/O by using a 4:10 Gearbox IC as shown in Figure 4 b).



**Figure 4:** 100Gb/s Ethernet Optics block diagrams: a) 100GE-SR10 parallel MMF with CAUI electrical I/O, b) 100GE-SR10 parallel MMF with CAUI-4 electrical I/O.

An extension of the 100GE-SR10 application is break out of the parallel MMF cable into ten duplex MMF fiber pairs to enable high 10GE-SR front panel density. 10x10G electrical I/O can directly support this functionality. However, CAUI-4 electrical I/O does not support this because it breaks up 10GE lanes into 5G Virtual Lanes. To preserve 10GE lanes, the OIF is defining a Multi Link Gearbox (MLG) standard [4] which will support 10:4 multiplexing and 4:10 de-multiplexing of ten 10GE asynchronous streams across a 4x25G electrical I/O interface.

## 10. Summary

CFP2 and CFP4 are two next generation 100G form factors. When introduced, they will double and quadruple front panel port density compared to the existing CFP form factor. This is enabled by advances in optics and IC integration, and increase in electrical I/O rate from 10G to 25G.

## 11. References

- [1] CFP Multi-source Agreement Documents. (<http://www.cfp-msa.org/documents.html>)
- [2] IEEE 802.3ba 40Gb/s and 100Gb/s Ethernet Task Force public area. (<http://www.ieee802.org/3/ba/index.html>)
- [3] IEEE 802.3 Next Generation 100Gb/s Optical Ethernet Study Group public area. (<http://www.ieee802.org/3/100GNGOPTX/public/index.html>)
- [4] OIF current projects public area. (<http://www.oiforum.com/public/currentprojects.html>)