A Simple Circuit-Level Model of Vertical-Cavity Surface-Emitting Lasers Working Over a Broad Temperature Range

Krzysztof Szczerba(1), Chris Kocot(1), Gary Landry(2)

(1) Finisar Corporation, 1389 Moffet Park Drive, Sunnyvale, CA 94089, USA, corresponding author: krzysztof.szczerba@finisar.com

(2) Finisar Corporation, 600 Millennium Drive, Allen, TX 75013, USA.

Abstract

In this paper, we present a simple circuit-level VCSEL model working over a broad range of ambient temperatures, while accounting for self-heating effects. We present the static, dynamic small signal and dynamic large signal performance compared to measurement results.

Introduction

The optical interconnects industry is currently moving to multi-level modulation, namely 4-level Pulse Amplitude Modulation[1] (PAM4). Short range optical links were historically built with directly modulated Vertical Cavity Surface Emitting Lasers (VCSELs), as they offer high modulation speeds at low energy consumption per bit, which is important in many applications, including megascale data centers. Therefore, new generations of VCSELs will likely dominate the short links in the coming years.

However, operation of PAM4 with VCSELs poses new challenges in understanding the VCSEL linearity, driver design and laser packaging. These tasks cannot be reliably performed based on the static performance and measured S-parameters of the VCSEL, as S-parameters do not capture the non-linearity of the devices. Volterra series-based device models are commonly used to model non-linear electronic components; however, they have limited support in measurement systems and circuit simulators. Therefore, circuit-based VCSEL models based on the laser rate equations were developed, including one by P. V. Mena[2,3].

In this paper, we present a similar rate equation-based circuit-level model that focuses on the simulation results, as well as a verification of the model against measurement data to verify the model operation.

A simple circuit-level VCSEL model

The circuit level model of the VCSEL is illustrated in Fig.1 and has four main parts: 1) the input RC network, 2) the network modelling the charge accumulation, 3) the network modelling the photon accumulation, and 4) a voltage source proportional to the optical output power. The voltage at the node *n* is proportional to the carrier density, whereas the voltage at the node *m* is proportional to the photon density in the cavity. The input network contains only one resistor, demonstrating the resistance of the DBR mirrors. The resistance of the junction is modelled using a controlled voltage source U_J. The DBR and the junction resistance are current and temperature dependent. The total internal temperature is dependent upon the ambient temperature and self-heating, which is a function of the bias current. Under an approximation that the temperature rise due to self-heating is the same at a given bias current for all ambient temperatures, the input resistance can be easily shown as a function of the ambient temperature and bias current. The input network also demonstrates the pad capacitance (C_p) and junction capacitance (C_p), with junction capacitance being a function of both temperature and current. Both the parameters of the input network and their dependencies were extracted as a fit to the measured S(1,1) parameters of a VCSEL. The charge carriers network, built around the node *n,* comprises a current source modelling the carriers injection, $I_{inj}=\eta_{int}\cdot I_a$, where

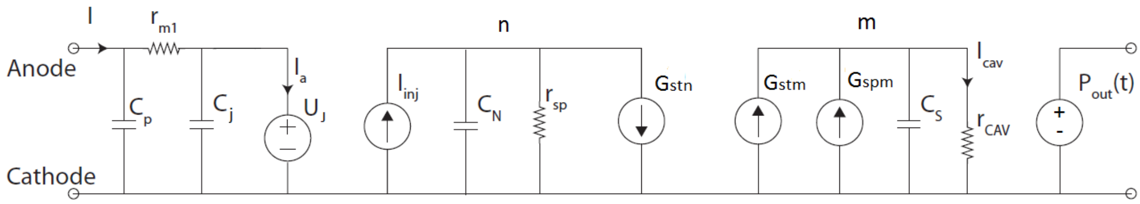

Fig. 1: A schematic representing the circuit level VCSEL model

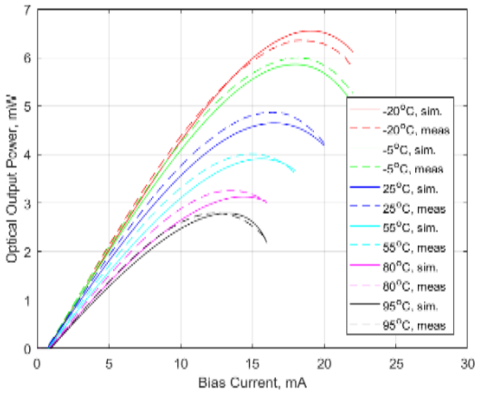

Fig. 2: Optical DC output power as a function of the bias current, simulated (solid) and measured (dashed) for temperatures ranging from -20°C to 95°C

η_{int} is the internal quantum efficiency and is temperature dependent. The capacitance C_N and the resistance r_{sp} are chosen so they yield a time constant equal to the carrier lifetime. The current source G_{stn} models carrier loss due to stimulated emission. The current source G_{stm} models the stimulated emissions of photons into the cavity and the source G_{spm} models the spontaneous emission. All of these current sources are temperature dependent. The time constant of the RC network at node *m* is chosen to correspond to the photon lifetime in the cavity. The optical output power represented by voltage P_{out} is proportional to the current through r_{cav} scaled by the optical output efficiency, which is also temperature dependent. The VCSEL parameters were extracted from LIV and S-parameter data that were measured using the method reported by J. C. Cartledge[4], except the input network was de-embedded using the fits to the S(1,1)

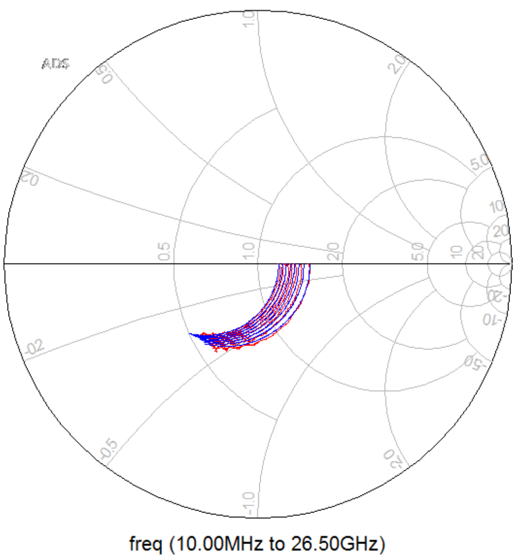

Fig. 4: S(1,1) parameters of the VCSEL, simulated in blue, measured in red at 80°C, for bias currents from 4 mA (rightmost) to 18 mA (leftmost) with a step of 2 mA.

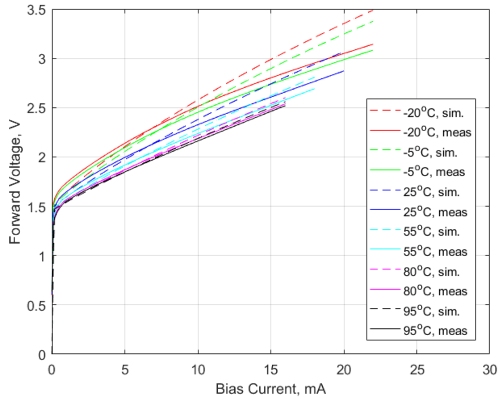

Fig. 3: Voltage across the VCSEL as a function of the bias current, simulated (solid) and measured (dashed) for temperatures ranging from -20°C to 95°C

parameters.

The self-heating network is not shown, as it is assumed that the thermal resistance is temperature dependent, based on the results presented by P. Baveja[5]. Additionally, it was shown that the main role in the thermal rollover is played by the decrease in the internal quantum efficiency due to the increased leakage. Therefore, the internal quantum efficiency was extracted from static LI measurements for the entire measured range of the bias current. The temperature was calculated using the ambient temperature, while the self-heating was calculated using the thermally dissipated power and known thermal resistance.

The model differs from those presented by P.V. Mena[2,3] in that the network part modelling the photon accumulation were not transformed in any way to improve the convergence. The convergence was instead assured by use of proper boundary conditions in the circuit components.

DC simulation results

The DC simulation results and their comparisons with measurements are presented in Fig. 2 and Fig. 3. The data is presented for temperatures of -20, -5, 25, 55, 80, and 95°C. Although better fits can be obtained by fitting all the VCSEL parameters at one ambient temperature, the strength of this model is proven in the fact that the same model can be used for temperature sweeps.

Most importantly, the model handles the threshold current and temperature rollover very well, at least to the point where the simulation gives a good estimate of the rollover current.

The IV characteristics, shown in Fig. 3, match

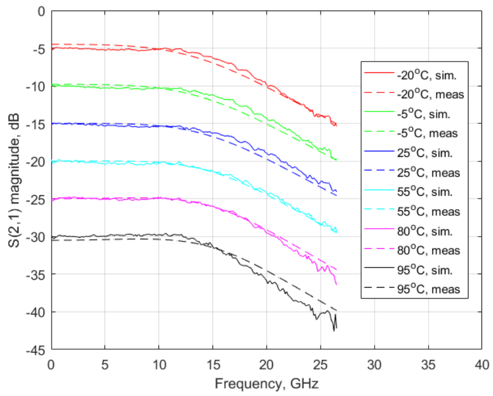

Fig. 5: S(2,1) parameters of the VCSEL, simulated (dashed lines) and measured (solid lines) at a bias current of 10 mA for temperatures between -20°C and 95°C. The plots are artificially offset in magnitude for improved readability.

well for higher ambient temperatures, but fall short in accuracy at higher bias currents at sub-zero temperatures, where the measured differential resistance drops significantly at higher bias currents.

Small signal simulation results

The small signal performance of the model was characterized with the S-parameters. The input impedance of the VCSEL is characterized using the S(1,1) parameters shown in a Smith chart, Fig. 4. The S(1,1) was simulated at 80°C for bias currents in the range of 4 mA to 18 mA with a 2 mA step. The simulation results are shown in blue and the measurement results are shown in red. The simulation correlates well in both amplitude and phase with the measurement, which is critical if the model is used for driver circuit and package design.

The magnitudes of the VCSEL transfer function, characterized by the S(2,1) parameters simulated for a 10 mA bias current over temperatures in a range between -20°C and 95°C are shown in Fig. 5. Again, the simulated response matches well with the measured response.

Large signal simulation results

The small signal characteristics are not sufficient to predict the large signal performance of the VCSEL, as the small signal S-parameters do not capture the non-linear behavior of the device. A large signal simulation of OOK at 28 Gbps was performed to verify the large signal dynamics of the model, and compared with measurement results. The simulations and measurements were performed at a bias current of 8 mA and 5 dB extinction ratio for temperatures of 25°C, 80°C and 95°C. The results are shown in Fig. 6, with

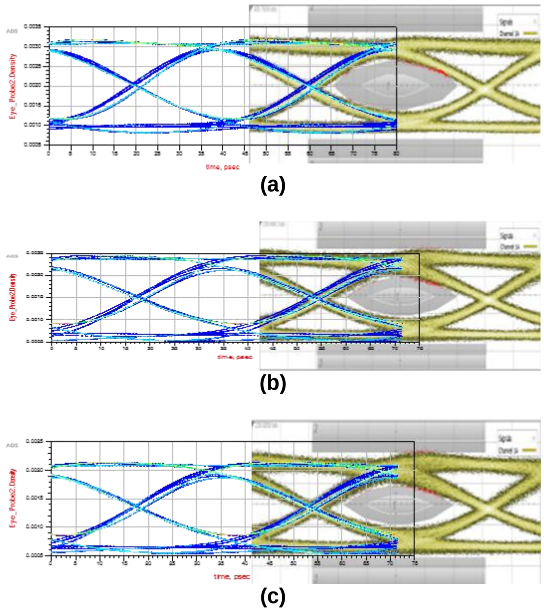

Fig. 6: Eye diagrams at 28 Gbps, 8 mA bias current at 5 dB extinction ratio, simulated (blue), and measured (yellow) for the following ambient temperatures: 25°C (a), 80°C (b) and 95°C (c).

the simulated and measured eye diagrams overlapped to show the correlation between the measurement and the simulation. The simulated large signal eye diagrams agree well in terms of rise and fall time, overshoot and deterministic jitter, and thus, the model is deemed to be sufficiently accurate.

Conclusions

We presented a circuit-level VCSEL model that is suitable for implementation in a circuit simulator. The model shows a good correlation with the experimentally measured parameters – both in the small signal and the large signal regime – over a range of temperatures from -20°C to 95°C. The DC operation was also shown to model the correct VCSEL behavior.

References

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